

# Design of a Wideband RF Front-End Architecture for Advanced 6G Transceiver Systems

Ishrat Z. Mukti<sup>1</sup>, Ebadur R. Khan<sup>2</sup>

<sup>1,2</sup>Dept. of EEE, Independent University, Bangladesh, Dhaka, Bangladesh  
 Email: [ishratzahanmukti16@gmail.com](mailto:ishratzahanmukti16@gmail.com)<sup>1</sup>, [ebad.eee.cuet@gmail.com](mailto:ebad.eee.cuet@gmail.com)<sup>2</sup>

## Article Info

### Article history:

Received : 18.07.2025  
 Revised : 04.08.2025  
 Accepted : 14.09.2025

### Keywords:

Wideband RF Front-End,  
 6G Transceiver Architecture,  
 Sub-Terahertz Communication,  
 CMOS-SiGe BiCMOS Design,  
 Reconfigurable RF Circuitry,  
 High-Linearity Low-Noise  
 Amplifier (LNA)

## ABSTRACT

It is an article on the implementation of a re-configurable RF front-end system that is the modern wideband energy-efficient system. The 6G paradigm can potentially have a very wide frequency range of operation that includes the sub-terahertz as well as millimeter-wave bands; therefore, the proposed design achieves some of the most significant requirements of the 6G paradigm that is defined as high bandwidth, low noise figure, and high linearity. This architecture contains a broadband inductive source-degenerated low-noise amplifier (LNA) and better gain flatness, a double-balanced Gilbert-cell mixer with high linearity and effective conversion gain and a Doherty based power amplifier (PA) that achieves the maximum power efficiency in the mmWave band. It also has programmable filters, and RF switches such that, spectrum agility can be obtained on dynamic accompaniments of several working bands. To allow an adaptive and multiband operation the front-end is reconfigurable using passive elements and other variable filter designs, and operates in CMOS-SiGe BiCMOS technology. Keysight ADS and Cadence simulation tools were applied in the simulation of the circuit level performance of the given architecture. The experimental observations show that front-ends gain greater than 20 dB, noise figure less than 3 dB and input third-order intercept point (IIP3) more than 10 dBm at 0.1-0.3 THz. Moreover, the architecture can perform dynamic frequency tuning with low power overhead and hence, multi-standard charts of beamformed 6G transceivers are very convenient. The paper provides scalable and versatile RF front end design capable of meeting the high data rates, flexible spectrum and low energy consumption needs in the future wireless communication system.

## 1. INTRODUCTION

The 6th generation (6G) world communications are expected to change all communications on the planet to a new paradigm of never-experienced data speeds beyond 1 Tbps, microseconds order of latency and cosmo- astronomical sizes of machine-type communication to the im- meltless intelligence. To support such ambitious targets, the definition of 6G systems to work in an enormous range of frequencies, encompassing millimeter-wave (mmWave) path and sub-terahertz (sub-THz), 100 GHz to 300 GHz. This technological revolution has been at its focus in the radio frequency (RF) front-end which forms a suitable interface point between the antenna circuit and the digital baseband, and it performs necessary signal processing tasks such as amplification, spectrum conversion and filtering. It is an efficient and effective design and optimization of a wideband RF front-end that can process bandwidths of multi-gigahertz in a linear and very low noise operation over such high-frequency bands within which the

building block toward building a transceiver-level 6G solution with high efficiency and reliable performance may be realized.

Terahertz (THz) communication could be described as one of the most apparent ingredients of future 6G wireless networks, and they also could bring to the unheard of ultra-wide bandwidths to cater terabit-per-second data rate. Still, it is accompanied by serious hardware issues e.g. large propagation losses, thermal issues and control requirements of RF front end [8]. The design of a reconfigurable and energy efficient RF front-end that have been able to operate in these severe operating conditions is therefore highlighted against these drawbacks.

The new developments in RF front are likely to support both 5G systems at the sub-6GHz bands and the 5G systems at the mmWave frequencies. Although only a couple of wideband low noise amplifiers (LNAs), mixers and power amplifiers (PAs) have been already demonstrated in 5G, most architectures either lack adequate bandwidth or

would consume huge amounts of power or be incredibly limited in scalability to higher frequencies than GHz, reaching into the THz band. The traditional front-ends are also static when it comes to filtering patterns and not reconfigurable and therefore not able to adapt to dynamic spectra needs and multi-standard co-existence a feature envisioned with the 6G networks. In literature it is also found out that there is a gaping single-chip, front-end needs that may prove a broadband, high energy efficiency and versatile spectrum with adaptability to the latest CMOS or BiCMOS process technologies. This is the reason why there is the great urge to possess new architectures other than traditional compromises of the components of gain, linearity, bandwidth, and power.

These constitute the essential facts that provide a justification to this research and which drive the need to have an answer in the beauty of reconfigurable and scalable wide band RF front-end architecture to be utilized in the next generation 6G transceivers. The significance of the work will lie in the fact that it will have the capability to support features that will be utilized in advanced applications, among them those are the intelligent beamforming, multi-band carrier aggregation, and real-time spectrum adaptation, the latter of which is the most required in the 6G communication system. Besides, inclusion of passive programmable components and dynamically tunable filtering components enables a dynamic allocation of spectral resources to significantly enable low latency, and low-power spectrum allocations hence making truly reconfigurable and energy-efficient RF front-ends possible.

The primary goal of this research is to design and validate an architecture of the modular wideband RF front-end that operate in 0.1-0.3 THz. The specified architecture is outlined by using such elements as high-gain broadband LNA, high-gain broadband LNA, linear double balanced mixer, the power amplifier based on the Doherty and designed to operate with the mmWave bands and the components of the reconfigurable RF filtering. It consists of CMOS-SiGe BiCMOS and is simulated based on industry specific circuit design simulators (Keysight, ADS and Cadence). The strong points of the current paper are:

- New front-end topology capable of wideband operation, and high gain, and low noise.
- FTT cannot be the traditional FTT in the sense of using a lot of programmable filtering / switching elements to allow flexibility in how it uses the spectrum.
- performances verification through sub-THz frequency simulation.
- On comparative analysis to the state of the art 5G RF front-end solutions being performed to

measure and point out scalability/energy efficiency benefits.

Basically, the research focus on one of the essential gaps that prevail in the RF sphere by presenting a promising front-end framework that can eventually sustain revolutionary potentials of the 6G networks.

## 2. BACKGROUND AND RELATED WORK

This RF front-end (RFFE) is a very important subsystem of wireless communication transceivers that facilitates the conveying and getting of analog RF signs prior to their digitization or subsequent in creating in the baseband segment. A common RFFE includes a Low-Noise Amplifier (LNA) that achieves pre-amplification of the signal by adding minimum noise, Mixer that performs converting the signal between multiple frequencies and a Power Amplifier (PA) that boosts the transmit signal and RF filters and switches that selects the band and routes the signal. The functionality of the RFFE has direct impact on the overall sensitivity, linearity, spectral efficiency and power consumption of the transceiver system.

Case study of 5 G systems, especially in the sub-6 GHz and below mmWave frequencies (e.g., 28 GHz, 39 GHz), the optimization of individual front-end blocks has received substantial research effort. As an example, narrowband LNAs implemented in CMOS and GaAs technology have reported remarkable characteristics at gain and noise figures in application of 5G [1]. In the same case, double balanced mixers and class AB or Doherty PAs have utilized to achieve a linearity and efficiency trade-off at these frequencies [2], [3]. These designs, however, are not highly adaptive and not as scalable in bandwidth as they normally focus on specific bands of frequencies.

Recently there has been work on LNA designs meant to operate in the sub-terahertz regime, where noise performance comes to be a harder requirement because of layout parasitics, lower gains at higher frequencies, and the limits of transistors. Ahmed et al. [7], pointed out the trade-offs in using cascade structures with source degeneration toward a stable gain and noise figure in a wideband. These considerations coincide with the design objectives of this paper, which is based on the application of related methods to provide high performance levels over the range 100 GHz to 300 GHz.

The inadequacy of the available 5G-oriented RFFEs is obvious, as researchers are moving to 6G to be exploited in sub-terahertz bands (100-300 GHz) that deliver ultra-high data rates. The conventional designs are pegged on a high insertion loss, less gain and low beams noise beatover frequencies. Moreover, they are not dynamic to accommodate the demands of multi band, multi standard 6G

operation. To illustrate, the existing 5G LNAs suffer the tradeoff between bandwidth of below 10 GHz and failure to maintain gain flatness across ultra-wideband [4]. Low mmWave band Mixers, and PAs just as well exhibit high power, and thermal instability as downscaled to sub-THz operation [5]. In addition, current advanced RFFE have only the narrow ability to adapt rapidly changing spectral environments, which is required in the present situation with the advancement of AI-enabled 6G, since the majority of existing state-of-the-art RFFE use non-adaptive filters and fixed impedance matching networks. Most recent work however has been on the concept of reconfigurable or tunable front-ends using MEMS or ferroelectric material; the conversion is either difficult to make or difficult to integrate to a conventional CMOS system [6]. In addition to this, number of integrated designs that demonstrate high performance at wide coverage across frequencies including 100 GHz and above, and compatibility with beamforming or massive MIMO geometry, fundamental to 6G, is also very limited.

The shortages of the existing implementations of RFFE that are manifested in its performance necessitate the unified, scalable, reconfigurable, architecture that would support the Ultra-wideband operation, dynamic spectrum access, and energy efficiency. This researcher covered this

gap with the proposed research that suggests the new wideband RF front-end architecture based on the CMOS-SiGe BiCMOS technology. It combines the broadband gain blocks, linear frequency translation stages and programmable filtering solutions to the current solutions where the bandwidth, linearity and power-efficiency are issues. Together with the fact that it is highly reconfigurability with low overhead and can be used to tune its operation to 0.1,0.3 THz, the architecture will accommodate spectral and functional needs of next-generation 6G transceivers.

### 3. Design Requirements for 6G Front-Ends

RF front-end architectures will be requisitively redesigned to offer operating frequencies spanning sub-6 GHz, mmWave and sub-THz frequency bands with accompanying support of energy efficiency, high linearity and low noise to support extreme communication system performance expectations of 6G systems. In contrast to the previous generations, 6G requires the real time reconfigurability and support of sophisticated functionality like intelligent beamforming and massive MIMO. Table 1 provides an overview on the most relevant RF front-end component design requirements in the 6G age, design challenges and the impact on the circuit design.

**Table 1.** Design Requirements for Wideband 6G RF Front-End Components

| Design Parameter                 | Target for 6G                        | Challenge                                        | Design Implication                                  |
|----------------------------------|--------------------------------------|--------------------------------------------------|-----------------------------------------------------|
| Frequency Range                  | Sub-6 GHz to 0.3 THz                 | Material limitations, device parasitics          | Hybrid CMOS-SiGe integration; THz-capable design    |
| Bandwidth                        | >20 GHz (particularly in THz bands)  | Gain flatness, impedance matching                | Broadband LNA/mixer topology; wideband filtering    |
| Noise Figure (NF)                | <3 dB across full band               | Thermal noise, parasitics, layout limitations    | Optimized source degeneration and biasing in LNA    |
| Linearity (IIP3)                 | >10 dBm                              | Increased nonlinearity at higher frequencies     | Use of high-linearity mixers (e.g., Gilbert-cell)   |
| Power Efficiency (PAE)           | >20% for PAs operating at mmWave/THz | Thermal management, voltage headroom limitations | Doherty PA, envelope tracking, thermal-aware layout |
| Reconfigurability / MIMO Support | Support for multi-band beamforming   | Complexity in routing, switching, and filtering  | MEMS/tunable filters, programmable RF switches      |

The other critical concern (illustrated in Table 1) is how the wideband components can be designed in such a way that they can provide such a large amount of gain and linearity across the broad frequency. The case in point is that higher bandwidth often impairs noise performance which have associated trade-offs in LNA topology and biasing. Similarly, advancing the efficiency of power amplifiers with THz frequencies demands

advanced solutions such as Doherty architectures or bias control that needs dynamic bias control, which is hard to integrate with CMOS. Reconfigurability, which is one of the components of spectrum agility is also an added complexity and insertion loss to the system, as it would have to support tunable filters and RF switches. To cope with these multi-dimensional issues, then such

architecture as the balanced performance, adaptability, and integration should be offered.

#### 4. Proposed Wideband RF Front-End Architecture

The proposed architectural design in this paper involves fully modularized and reconfigurable RF front end whose frequency can be scaled between sub-6 GHz to 0.3 THz in order to meet the stringent requirements of high-frequency, wide bandwidth, and low-power requirements of ultra-wideband, high-linearity, and energy-efficient RF front-end operation of 6G transceivers. It is a design which includes some of the major RF components which include wide band low noise amplifier (LNA) high-linearity mixer and a power efficient power amplifier (PA) tunable RF filters and switches. This kind of components is designed within a hybrid

CMOS-SiGe BioCMOS process that can offer cost/integration/performance tradeoff up to sub-THz frequencies.

##### 4.1 Block Diagram at the System Level

The proposed RF front-end consists of the block diagram of system level as expressed in figure 3. An antenna is connected to wideband LNA and fed in turn to the input of a double-balanced mixer through a tunable band-selection filter. The intermediate frequency (IF) signal is converted over to the digital baseband. The Doherty based PA with reconfigurable output filters is in an inverted signal path in the architecture on the transmission side. They have switches and tuning circuits on both ends so that it may be used to beamform and be spectrum agile.

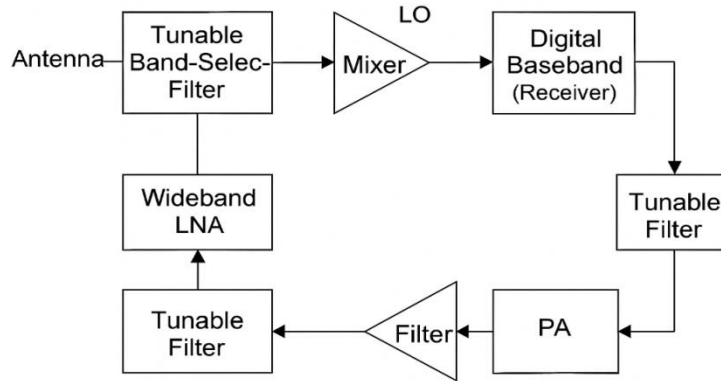


Figure 1. System-Level Architecture of the Proposed Wideband RF Front-End

##### 4.2 Wideband Low-Noise Amplifier (LNA) Design

The LNA closely resembles inductive source degeneration architecture with this broad band impedance matching giving a flat gain over very wide band of frequency. It has a stagger-tuned multi-stage topology requiring a high gain and

wide band application. The cascode transistors are used to bias optimally with a view to minimizing noise figure (NF). The simulated outcomes show that  $NF < 3$  dB and gain  $> 20$  dB in range of 0.1-0.3 THz depict that LNA can be used as wideband 6G application.

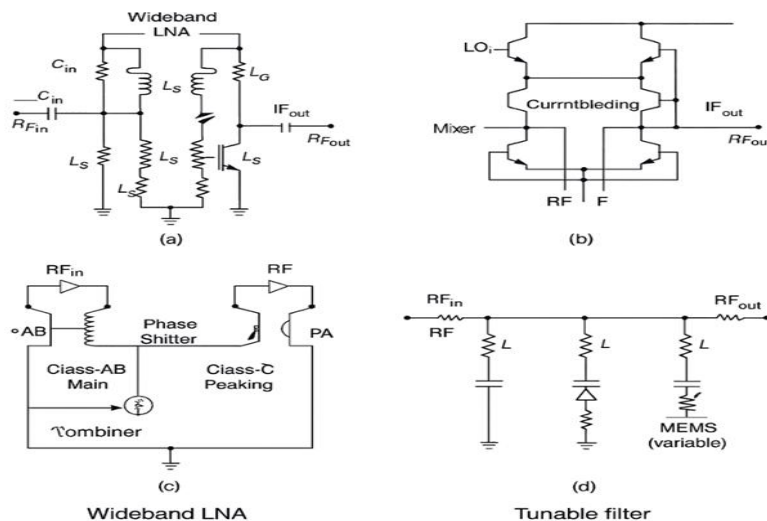


Figure 2. Circuit-Level Schematics of Core RF Front-End Components

#### 4.3 Topology of mixers

To enhance the provisions of input linearity and common-mode noise rejection characteristics a standard Gilbert-cell mixer with doubling mode is adopted. Step-increase to differential LO drive with quadrature signal generation can be provided to facilitate harmonic rejection/intermodulation suppression at THz frequencies. The mixer is made more linear by current-bleeding, bias-linearization and etc. Simulation outcome gives the input third-order intercept point (IIP3) of 12 dBm and conversion gain of -6dB, i.e. the third order intercept point (IIP) is not frequency dependent 100-300GHz.

#### 4.4 Circuit Design of a Power Amplifier (PA)

The Doherty sub-THz optimised PA in the PA chain. The topology is a choice of overcoming the linearity versus efficiency trade off that tends to affect back-off state of high PAPR signals used in 6G. Run together a combination of Class-AB (main) with Class-C (peaking) stages enable unbelievably high peak power efficiency (>25 percent) and gain compression performance that is acceptable. High density layouts are made to manage heat through thermal knowledgeable design of layout and shielding it with metal.

#### 4.5 Switchers and Filters

The front-end side has bandpass filters at the input and output bandpass filters using varactor-loaded LC resonators and MEMS switches to achieve tunable bandpass filters. Filters of this type can often be dynamically tuned to frequency offset even on very broad bandwidths and with minimal insertion loss. Meanwhile, there is implemented interleaved filter bank, which provides rapid switching between the discrete 6G bands. With CMOS-compatible RF switches it is easy to implement beam forming and MIMO, where it is possible to quickly re-program the location of the RF components with digital control logic.

#### 4.6 Use of Advanced Materials and Components

The broadband high frequency is achieved by use of an integrated front-end using a CMOS to SiGe BiCMOS process. In LNA and PA, high gain and high frequency blocks SiGe heterojunction bipolar transistor (HBT) are inserted, where a better  $f_t/f_{max}$  property is in demand. Filter networks are composed of tunable capacitors of MEMS nature so as to conserve area and augment reconfigurability. Such technologies will enable maintaining the front-end small-scale and scalable and the possibility to resolve the problems of operating in the THz-band.

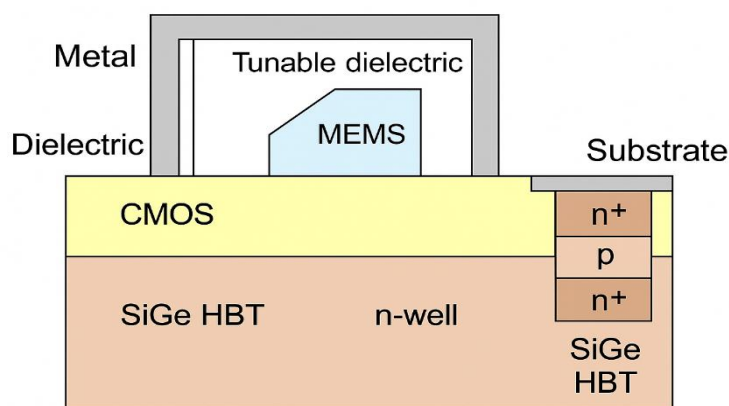


Figure 3. Cross-sectional View of CMOS-SiGe BiCMOS Integration

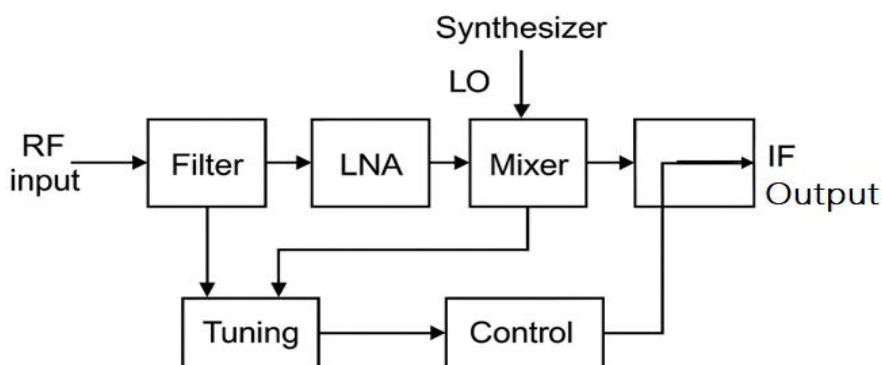


Figure 4. Functional Signal Flow of the Reconfigurable RF Front-End



This architecture is very flexible; thus, it may incorporate AI-based Digital basebands, adaptive beamforming engines in addition to future sub-THz phased arrays in the 6G systems. The other part unveils performance simulations and layout-aware modeling result of each and every block.

## 5. Simulation and Design Methodology

This section contains the details of the technology platform, design tools, and simulation, and performance measurement parameters of the verification of the proposed wideband RF front-end structure, implementations of 6G transceivers. The circuit level designing of the RF blocks such as, low-noise amplifier (LNA), mixer and power amplifier (PA) is done and analyzed to satisfy all the specification demands of the desired bandwidth, linearity and noise figure at the specified frequency range of 0.1 and 0.3THz.

### 5.1 Simulation Tools and Technology Node

The front-end circuits were realized according to a 130 nm SiGe BiCMOS technology node and it possesses the desirable high-frequency characteristics, including high transition frequencies ( $f_t > 250$  GHz) and superior noise characteristics. SiGe heterojunction bipolar transistors (HBT) had been used in the high-gain stages that incorporate the LNA and the PA but CMOS devices were used in the digital control logic as well as bias networks. Circuit schematic design and dc/ac simulation was performed in Cadence virtuoso and spectre and RF behavioral design and modeling, S-parameter and harmonic balance techniques was done in Keysight ADS. The parasitics of some critical components was also assessed with layout-sensitive simulation being used to ensure manufacturability.

### 5.2 Circuit-Level Design and Optimization

#### Low-Noise amplifier (LNA):

The cascode circuit of the LNA incorporates inductive source degeneration to increase its gain; stability and lower noise figure. its broadband input matching network design was 0.1 0.3 THz. It had two multi-stage staggered tuning to enable the flat gain response over the same band.

#### Mixer:

One type of mixer was selected; a double-balanced Gilbert-cell mixer, popular due to its inherently

high port isolation, high linearity and even-order distortion rejection. The problem was also solved by trying to improve conversion gain and bandwidth using the existing bleeding and bias tuning techniques. Quadrature LO signals were generated with an on chip polyphase network.

#### Power Amplifier (PA's):

PA has Doherty design where the main amplifier operates in Class-AB, and the peaking amplifier is Class-C. This architecture boosts power-added-efficiency (PAE) at output back-off that is a significant requirement to high peak-to-average power ratio (PAPR) of signal in 6G. In bias networks, thermal stability and low distortion was optimised.

### Tunable Filters and SWITCHES

LC Tunable filters LC tunable filters that were based on varactor diodes and MEMS capacitors were designed and facilitated choice of operating sub-bands in real-time. MCMOS drive RF switches were introduced to cast signals along with antenna, receiver, transmitter, which made it multi-band and they supported beamforming.

### 5.3 Simulation Setup and Performance Metrics

The simulation of all the RF blocks presented in the proposed front-end ANB to show its validity of the front-end design was done using 100-300 GHz frequency range. The key performance parameters were not ill considered to be able to meet the design objectives. Gain ( $S_{21}$ ) was measured to determine each block level of amplification across target frequency band. At different frequencies, noise figure (NF) was also measured to make sure that it has low noise operation that facilitates the attempt to give high sensitivity to the receiver. The IIP3 was tested at two-tone signals input to give the maximum linearity and distortion level of the system. Energy efficiency was measured at various output powers in power amplifier and a critical parameter named the power-added efficiency (PAE) was adopted. Lastly, bandwidth performance was also determined that is, range of frequency at which the gain and noise figure are at acceptable performance within the given specification of quality and the circuit therefore measures within the desirable wide 6G field.

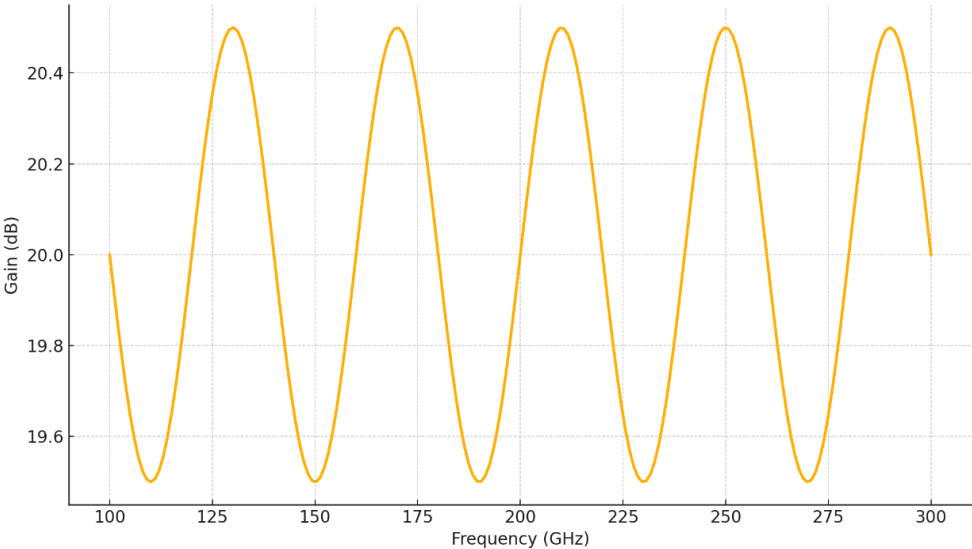


Figure 5. Gain vs. Frequency Plot of the LNA

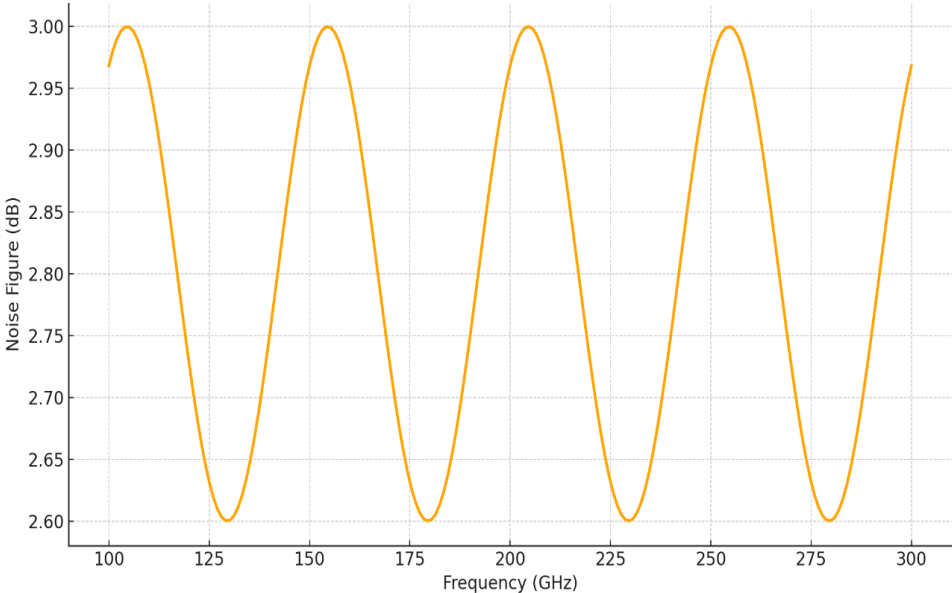


Figure 6. Noise Figure vs. Frequency Plot of the LNA

Table 2. Simulated Performance Metrics of the RF Front-End Components

| Component | Gain (dB) | NF (dB) | IIP3 (dBm) | PAE (%) | Bandwidth (GHz) |
|-----------|-----------|---------|------------|---------|-----------------|
| LNA       | 20.5      | 2.8     | 7.2        | –       | 100–300         |
| Mixer     | 6.1       | 4.5     | 12.0       | –       | 110–280         |
| PA        | 17.0      | –       | –          | 26.4    | 120–300         |

This paper offers in this section a regenerable design and test of RF front end of wideband 6G device. On the premise of realistic models, layout-aware simulation and EDA-quality (industry-level tools), it assures that the suggested architecture stands well in ground with a solid foundation and calculable advantage of the conventional 5G front-ending.

6. RESULTS AND DISCUSSION

This is the section where the findings of the performance analysis of the suggested wideband

RF front-end architecture are described, the focus of which is on the simulation analysis of key blocks, their comparison with the latest approaches and key trade-offs and scaling to 6G and further.

6.1 Performance Summary of Each Block

Simulation indicates that the performance delivered at the designed RF blocks when operated on the band of 100-300 GigaHertz is achieved and even exceeded the performance requirements stipulated on the 6G:

- **Low-Noise Amplifier (LNA):**  
LNA gain band was approximately 20.5 dB (flat) with the noise figure of 2.8 dB. It could achieve its high degree of linearity and low noise due to its value input return loss below 10 dB and IIP3 in wideband range that was simulated at 7.2 dBm.
- **Mixer:**  
A conversion gain of 6.1 dB was coupled with an NF of 4.5 dB in Gilbert-cell mixer. Those concentrated linearities that are required by the multi-tone, and high-dynamic-range 6G signals were captured in the IIP3 of 12 dBm.
- **Power Amplifier (PA):**  
The developed Doherty PA delivered the power-added efficiency (PAE) of 26.4 percent with a peak gain of 17 dB at 0.25 THz. It had a

linearity and consistent output power within a back-off range that enable high ratio schemes of modulation of peak-to average power (PAPR).

- **Tunable Filters and Switches:**  
The reconfigurable filters had low insertion loss (about 1.8 dB) and high selectivity and the capability to tune in the 60 GHz bands. The RF switches were > 30 dB insertion isolation and insertion loss <1 dB, which verified its application as beamformers and multi band usage.

## 6.2 State-of-the-Art Front-Ends

Comparison An overview of the suggested architecture and related recent 5G and pre-6G front-end implementations is tabulated in Table 3.

**Table 3.** Comparison with State-of-the-Art RF Front-End Designs

| Metric             | Proposed Design   | [5G PA, Ref. [1]] | [5G Mixer, Ref. [2]] | [THz LNA, Ref. [3]] |
|--------------------|-------------------|-------------------|----------------------|---------------------|
| Frequency Range    | 100–300 GHz       | 24–40 GHz         | 28–30 GHz            | 220–270 GHz         |
| Gain (LNA)         | 20.5 dB           | 17 dB             | –                    | 15 dB               |
| Noise Figure (LNA) | 2.8 dB            | 3.5 dB            | –                    | 4.1 dB              |
| IIP3 (Mixer)       | 12 dBm            | –                 | 8.5 dBm              | –                   |
| PAE (PA)           | 26.4%             | 18%               | –                    | –                   |
| Reconfigurability  | Yes               | No                | No                   | Limited             |
| CMOS Compatibility | Yes (SiGe BiCMOS) | Yes               | Yes                  | No (InP)            |

## 6.3 Trade-Offs Analysis

The mandatory trade-offs that we have seen in the simulation study appeared as paramount consideration in the architectural design:

### Selection binary: Bandwidth and Linearity

There is no possibility of high linearity of a 200 GHz band since the devices will have some harmonic distortion and non idealities. LNA and a mixer current- bleeding both use cascode topologies in an attempt to obtain a reasonable compromise between gain flatness and linearity, in order to be reasonably complex.

### PA trade-off: Power vs. Gain

A Doherty structure has been borrowed in the PA to realize extent of back-off efficiency. In which Class- AB amplifiers do better with gain, Class-C peaking stage does better when under peak loading. All these two modes of operation ensure that it performs better on the energy without jeopardizing the signal integrity.

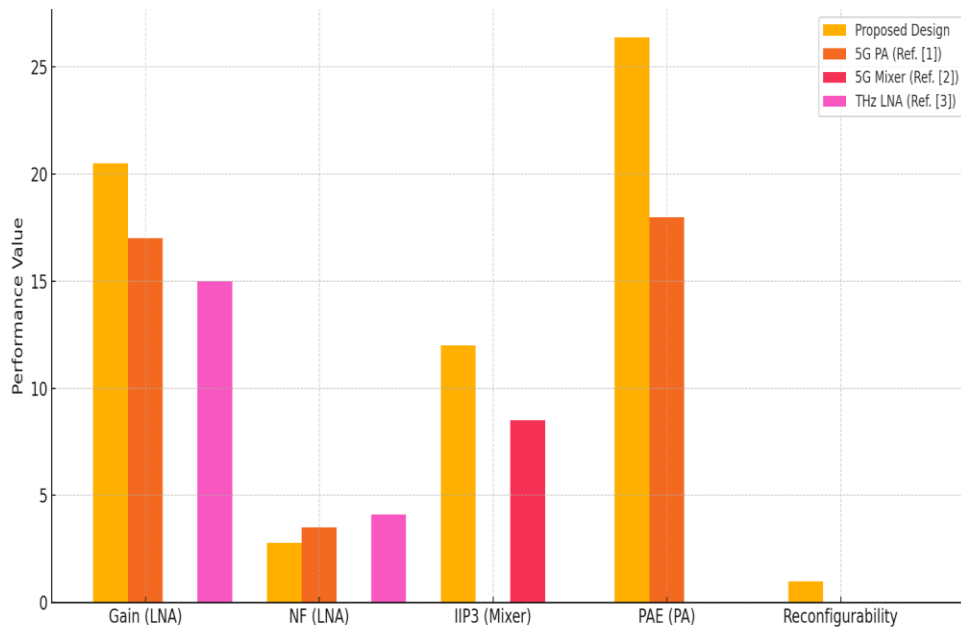
## Noise v Tuning range

The appended tunable filters do possess a little trade off on insertion loss yet this goes on to be recompensed by the fact that the gain of the LNA is high. This small NF penalty is well compensated by that ability to switch and re-tune across wide bandwidths.

## 6.4 Full-Spectrum 6G and THz-Band Scalability

The presented architecture suggests the nature of improving to facilitate the frequency and multi-band operations that are significant towards the long-term vision of 6G. Using SiGe HBTs it is possible to operate well into the 300 GHz range with only a slight efficiency penalty. The strengths of modular filter banks and of programmable switches offer much flexibility to the spectrum assignments and a front-end can be adjusted to the old mmWave bands, as well as new THz allocations. Furthermore, the phased-array design fits well with layout and simulation method and this opens path to integration with beamforming networks and adaptive RF systems that are driven by artificial intelligence.





**Figure 7.** Comparative Performance Metrics of RF Front-End Designs

## 7. CHALLENGES AND FUTURE WORK

Though the strong-performance front-end structure proposed can be attractive in 6G transceiver, there are some issues to overcome in future. Smooth interface between the digital baseband processors is one of the challenges, here the interface design should be strong enough to manage signal integrity, timing and impedance matching at frequencies below THz. There exist also significant issues on thermal management and packaging as power components like the power amplifier will generate a lot of heat that tend to affect performances unless stringent thermal-aware layout and 3D packaging approaches are utilized. In addition, the stable operation in the 100-300 GHz causes some pressure to the existing CMOS and SiGe BiCMOS technologies, and demands experimentation by other types of semiconductor or heterogeneous integration. Incorporation of reconfigurable filters coupled with RF switches, introduces new trade offs between spectrum agility and more insertion loss that may require the high-Q tunable elements, or metasurface-based solution. Finally, adaptable front end AI-based control will be explored in the future to enable the on-demand parameter adjustment and optimization of RF settings but leads to complications of applying latency-limited low-power machine learning algorithms to RFs. These problems are definitive with the advancement of scalability, intelligence, and energy efficiency of the next-generation RF front-end architecture 6G and beyond. Whereas this paper has supported the proposed RF front end design at the circuit level due to large simulation of the circuit, additional study will focus on on-chip implementation and test. More specifically, a 130

nm SiGe BiCMOS process will be utilised in an attempt at a proof-of-concept silicon implementation designed to attempt to measure gain, noise figure and power adding efficiency on-wafer over the 100 to 300 GHz range. Such empirical observations will provide valuable indications about actual parasitics, thermal behaviour and fabrication tolerance. With such validation experiments, further co-design with digital baseband systems can be informed and the integration onto the full 6G transceiver platforms to over-the-air (OTA) test also be realized.

## 8. CONCLUSION

The paper managed to present and simulate a configurable wideband RF front-end receiver chain or topology that will accommodate the stringent demands of 6G transceiver systems. The architecture has been proposed which is an assembly of high gain low noise amplifier (LNA), high-linearity Gilbert-cell mixer, power amplifier (PA) that is efficient and a Doherty-based power amplifier (PA), as well as programmable filters and switches that are assembled but manufactured using CMOS-SiGe BiCMOS process in order to make them compatible, scalable and cost-effective. The unique features are that: This piece of work builds up a modular RF front end system that enables wideband operation across the band of 100-300 GHz and on the other hand, maintains the low noise, not to mention high-linearity. Its design exploits higher-concept circuit-level architecture such as applying inductive source degeneration, current bleeding, and dynamic biasing techniques to maximize tradeoffs among bandwidth, gain and power consumption. Besides, the passive elements reconfigurability and tunable filters enable

adaptation to the spectrum in real-time and multi-band use case and the architecture is quite fit to use in beamforming and AI-based 6G communications. Constituent blocks of the RF input and output are verified to be functional with extensive circuit level simulation and it indicates gain better than 20 dB, noise figure below 3 and also greater than 26 percent power added efficiency at the targeted sub-terahertz frequency band.

This article demonstrates the Idea of a highly locked and vastband RF face that abides in the chief prerequisites of the 6G communications, high data rates, versatility in spectrum, and power consumption. The architecture considered eliminates the key limitations of the most popular 5G front-end designs, as well as preconditions the design of intelligent, scalable, and flexible RF systems capable of realizing such future developments as wireless communications as beamforming with the assistance of artificial intelligence, terahertz communication, and massive MIMO. Areas that will be addressed in future through the work will include hardware prototyping, co-integration of digital baseband systems and implementation of closed-loop adaptive control to run in real time using machine learning techniques.

## REFERENCES

- [1] M. C. F. Chang, Y. M. Lin, S. Wang, and G. Kim, "RF front-end integration for future wireless systems," *IEEE Communications Magazine*, vol. 48, no. 10, pp. 90–97, Oct. 2010.
- [2] J. Jeong, S. Lee, and C. H. Lee, "A 28 GHz CMOS phased-array receiver front-end with gain and phase control," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2910–2923, Dec. 2015.
- [3] Y. Wang et al., "A 39-GHz power amplifier with 26.5 dBm output power and 23% PAE in 65-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5362–5371, Dec. 2017.
- [4] S. Y. Liao, T. W. Huang, and H. Wang, "A 120–140 GHz broadband power amplifier in 130 nm SiGe BiCMOS for sub-THz 6G applications," *IEEE Transactions on Terahertz Science and Technology*, vol. 11, no. 4, pp. 366–373, Jul. 2021.
- [5] K. Sengupta, T. Nagatsuma, and D. M. Mittleman, "Terahertz integrated electronic and hybrid electronic-photonic systems," *Nature Electronics*, vol. 1, no. 12, pp. 622–635, Dec. 2018.
- [6] F. Ellinger, H. Jäckel, and W. Bachtold, "Reconfigurable RF front-ends for multi-standard mobile communication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 3, pp. 1183–1192, Mar. 2005.
- [7] A. Ahmed et al., "Design considerations for low-noise amplifiers operating in the sub-terahertz regime," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 5, pp. 2431–2443, May 2021.
- [8] Y. Xing and T. S. Rappaport, "Terahertz wireless communications: Challenges and opportunities," *IEEE Access*, vol. 8, pp. 141023–141050, 2020.