Electronics, Communications, and Computing Summit
Vol. 3, No. 3, Jul - Sep 2025, pp. 80-89
ISSN: 3107-8222, DOI: https://doi.org/10.17051/ECC/03.03.09

Implementation and Evaluation of Subthreshold Logic for Energy-Constrained IoT Devices

M.Karpagam[1], P. Sathish Kumar[2]

[1]Assistant Professor, Department of Computational Intelligence, SRM Institute of Science and Technology, Kattankulathur, Chennai, Email:karpist@gmail.com
[2]Assistant Professor, Department of computer science and Engineering, J.J College of Engineering and Technology, Tiruchirapalli

Article Info

Article history:

Received : 12.07.2025
Revised : 14.08.2025
Accepted : 20.09.2025

Keywords:

Subthreshold Logic,
Ultra-Low-Power Design,
Energy-Constrained IoT Devices,
CMOS Circuit Optimization,
Power-Delay Product (PDP),
Low-Voltage Digital Design

ABSTRACT

The ubiquity of Internet of Things (IoT) devices has highlighted the severe importance to design circuits with ultra-low-power with specific regard to applications in a low-energy environment e.g. in battery-operated and energy-harvesting applications. Performance-efficient, basic CMOS logic-circuits tend to be inappropriate in such energy-constrained application because of excessive dynamic and stationary power requirements. Here subthreshold logic, in which transistors are driven below the threshold voltage, promises to allow significant power savings at the cost of slower switching speed. The research paper at hand is devoted to system designed and implemented low-power subthreshold logic circuits that are rational in IoT systems. We use a 65nm CMOS technology node on which to build a set of benchmark digital circuits, hypothetical elementary logic gates, adders and counters, and study their behaviour as they operate on subthreshold Vt. The design approach is related to the most important questions like sizing of the device with the help of leakage abatement and sensitivity to the process-voltage-temperature (PVT) variations. Analysis of key performance measures such as power consumption, propagation delay and power-delay product (PDP) can be simulated and hardware prototyped using industry-standard EDA tools. On experimental basis, subthreshold logic circuits have been observed to reduce power consumption by up to 90 percent, compared to super-threshold circuit designs, under typical workloads in the IoT domain, with no loss of functional correctness. These results confirm that energy-constrained embedded systems are feasible using subthreshold design and the future of improving energy-constrained embedded systems is through adaptive biasing and near-threshold techniques.

1. INTRODUCTION

The boom of Internet of Things (IoT) devices in wide-ranging applications (including environmental sensing, industrial monitoring, smart homes and biomedical bodies), has created rigid limits on energy use. A good percentage of these devices available work in conditions where they are not supplied with a great amount of energy resources, instead they depend on small batteries or the surrounding energy-harvesting methods. Consequently, reducing of power consumption proved to be an essential requirement to the realization of digital circuits of such embedded systems.

In that regard, energy-efficient logic design is instrumental to making battery lifetime much longer, alleviating the need to discharge batteries at all, and powering long-time autonomous operation. Conventional digital logic circuits usually perform at the super-threshold regime of transistors operation, and thus their dynamic and static power consumption is significant, unsuitable to ultra-low-power applications. As a solution to this problem subshow logic design has been put forward as a viable substitute. Transistors can work at supply voltages below their threshold voltages in subthreshold mode, greatly decreasing switching and leakage power. Although the cost of using such a method is in terms of lower performance and higher susceptibility to changes, it fits the low-computational and intermittent activity levels of the majority of applications within the IoT.

In this paper, I will discuss the implementation and assessment of subthreshold logic circuits that have specifically been tailored to the IoT systems with energy constraints. The research establishes the application of a 65nm CMOS technology node in

the design, simulation and analysis stage of various basic digital block units- logic gates, arithmetic units and sequential components- that function at the sub threshold region. The experiment intends to model the trade offs between energy efficiency and performance, and also to verify the feasibility of the sub threshold logic by performing extensive simulation based analysis.

The merits of the work are mainly the focus on the feasibility of using subthreshold logic circuits in the ultra-low-power internet-of-things applications. To begin with, the systematic design process is suggested with the 65nm CMOS technology to focus on the devices sizing and supply voltage requirements to realize the accurate subthreshold operation. The paper also entails a system-level deployment of exemplar benchmark circuits, specifically, logic gate, arithmetic processors, and sequential components to accommodate the peculiarities of the power-constrained IoT workload hero. The behaviour of these circuits is evaluated in details in terms of process-voltage-temperature (PVT) variations, resulting in the evaluation of their reliability and robustness in real-life conditions. Moreover, the side by side comparison is shown by running a thorough comparison of subthreshold and regular super-threshold design with regards to essential design performances such as power consumption, path delay, and power delay product (PDP). In sum, these discoveries confirm the usefulness of subthreshold logic as an attractive approach to energy-limited embedded systems and furnish a firm basis to future improvement of low voltage digital circuit design.

2. Background and Related Work

2.1 CMOS Power Dissipation Fundamentals

The total power consumption in CMOS digital circuits comprises three primary components: dynamic power, short-circuit power, and static (leakage) power. Dynamic power is the dominant component in active switching and is expressed by the well-known equation

$$P_{dynamic} = \alpha C_L V_{DD}^2 f \_\_\_\_\_ (1)$$

where α is the switching activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, and f is the operating frequency. As technology scales, leakage power—especially subthreshold leakage current—has become increasingly significant in deep submicron processes. This leakage is exacerbated by reduced threshold voltages, increasing the importance of energy-efficient circuit techniques in modern IoT designs [1].

2.2 Subthreshold Logic Principles

In subthreshold operation, the supply voltage V_{DD} is reduced below the threshold voltage V_{th} of MOS transistors. In this regime, the transistor operates in weak inversion, and the drain current I_D exhibits an exponential dependence on gate-to-source voltage V_{GS}, given approximately by

$$I_D \approx I_0 e \frac{(VGS - Vth)}{nV_T} \_\_\_\_\_ (2)$$

where I_0 is the process-dependent current, V_T is the thermal voltage, and n is the subthreshold slope factor. Although the switching speed is significantly reduced due to lower current drive, subthreshold operation can yield orders-of-magnitude reductions in power consumption, making it attractive for ultra-low-power applications [2], [3].

2.3 Previous Efforts in Subthreshold Digital Design

There are many papers that have investigated the possibility of subthreshold logic to low-energy computing. The subthreshold energy-efficient DSPs pioneered by Chandrakasan et al. note their applicability in portable electronics [4]. Calhoun and Chandrakasan offered the methods of robust development of SRAM working in subthreshold mode and discussed such issues as low operating voltage and read/ write margins [5]. Recent designs have been able to scale subthreshold design into microcontrollers and full system-on-chip (SoC) designs of biomedical and sensor applications [6], [7]. The workloads in these studies are real world whereas the energy savings claims are substantial as long as the performance demands are not extreme.

2.4 Limitations and Open Challenges

Subthreshold logic design has a couple of rather important limitations in spite of its promise. The propagation delays are high because current levels have been drastically reduced, which is the first reason that restricts the maximum operating frequency. Second, the circuits are highly process, voltage, and temperature (PVT) sensitive and this makes them hard to design robustly. The leakage currents, which are comparatively higher in the subthreshold make a problem as they are exponentially related to temperature and threshold voltage deviations. Furthermore, narrow noise margins and lower drive strength of subthreshold circuits makes timing closure and signal integrity more difficult. The present day research activities are experimenting with adaptive body biasing, dynamic threshold modulation and a combination of sub/near threshold architecture to address these problems [8], [9].

3. Design Methodology

In this section the strategy used with regard to implementation and evaluation of subthreshold logic circuits is described. Examples include the technology and tools, benchmark circuit selection,

subthreshold design-specific constraints and logic styles examined.

3.1 Technology and Design Tools

These circuits were optimized using a design-for-test methodology in subthreshold circuits proposed, and they were explored to work in a CMOS technology node (65nm) because it offered trade-offs between performance, leakage control, and availability through open-source and academic process design kits (PDKs). These simulation and design activities were carried out on Cadence Virtuoso in the drawing and layout design and spectre spice simulations conducted to evaluate the pre and post layout performance. Assura DRC/LVS tool was used to check the functionality and correctness with design rules. The simulation has been done at transistor level with the supply voltages varying and commencing at 0.2 with supply voltages as 0.5. This was to obtain the optimum operating voltage in the subthreshold operating regime.

3.2 Selection of Benchmark Circuits

To evaluate the effectiveness of subthreshold operation, a suite of benchmark circuits commonly used in low-power embedded systems was selected. These include:

- **Inverter Gate** – The fundamental building block used for parameter tuning and characterization.
- **2-Input NAND and NOR Gates** – To assess logical functionality under varying input transitions.
- **D Flip-Flop** – For analyzing sequential behavior and clocked operation under subthreshold supply.
- **4-bit Ripple Carry Adder (RCA)** – A representative arithmetic block for examining delay propagation.
- **4-bit Binary Counter** – Used to validate sequential logic under real-time operation scenarios.

Each benchmark was designed and simulated independently and then integrated into a small test system for functional validation.

3.3 Subthreshold Design Constraints

Subthreshold circuit designing puts a new set of challenges and requirements on the table and circuits need to be designed keeping in mind these new factors. Transistor sizing may be one of the major issues since in the subthreshold regime the current flowing through a transistor varies exponentially with gate voltage. Transistors, both PMOS and NMOS, are designed wider than typical designs to compensate for the intrinsically low drive current, and also to allow better performance and control of leakage. Another important factor is the threshold voltage; because the voltage V_{DD} is smaller than the threshold voltage Vth the transistors are in the weak inversion region. Although standard-V th devices in most cases may be used to tradeoff between performance and leakage, low-V th devices can be used selectively in performance-critical paths at the expense of increased leakage. In subthreshold designs leakage is a major problem and leakage current, though low, is still substantial. Standby power was mitigated through techniques like transistor stacking, reduction of leakage paths and adoption of power-gating techniques. Also, they applied high-V_{th} devices in non-critical paths in order to limit static power. To make the designs robust to process-voltage-temperature (PVT) variations, each of the designs was extensively simulated under different process corners (TT, SS, FF), voltage variations (10% above and below the nominal V_{DD}), and a broad temperature span (0^0 C to 85^0 C). All these limitations and considerations work in unison towards achievement of successful development of reliable and energy efficient subthreshold logic circuits.

3.4 Logic Styles Considered

This study has the baseline design designed in CMOS logic, which has the advantages of naturally immune noise, design speed, and faultless compatibility with the traditional EDA toolchains. Static CMOS type also provides full voltage swing, low static power, and consistent operation in a wide range of environmental conditions and this makes the type quite reliable in being used in subthreshold applications. Different styles of logic were checked as well to investigate possibilities of further energy improvement. Dynamic Voltage logic (DVL) was tested where reduction in switching energy was possible due to dynamic variations in voltage levels of special nodes. On the one hand, DVL has the potential to provide energy advantage; on the other hand it adds great design complexity, especially with respect to fine clocking and charge sharing among transistors. Also adiabatic logic was simulated as a theoretical model. Adiabatic circuits provide a mechanism to circulate and recapture the energy during switching by using slowly modulated power clocks but its usage in subthreshold mode is not widely adopted because of higher overhead in the design and difficulty of implementing multi-phase power. These trade-offs were used to decide on the primary implementation type of logic and a sole choice was made: static CMOS. Still, the discussion on the alternative styles outlined problems and solutions that can be used in the future improvement of the ultra-low-power circuit design.

Figure 1 shows the entire flow of design that was followed in the study, since the technology setup up to the logic style analysis and eventual implementation.

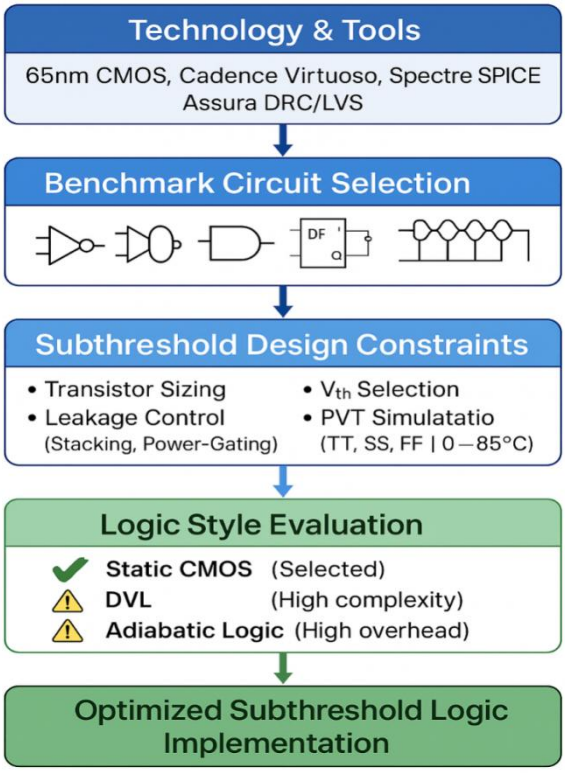


Figure 1. Design Methodology for Subthreshold Logic Circuit Implementation

Design methodology for implementing and evaluating subthreshold logic circuits. The flow illustrates the technology stack, benchmark selection, design constraints, logic style evaluation, and final implementation process.

4. Implementation

Here, the section recounts the realistic practice of subthreshold logic circuits, including the design of a schematic, layout issues, voltage feeding system, design confirm process, and the system technology in which physical design methods to reduce leakage.

4.1 Schematic and Layout Design

The implementation arose with the schematic realization of benchmark circuits at transistor level, such as simple logic gates, flip-flops and arithmetic circuits. The design of the circuits was done with the aid of 65nm CMOS process design kit (PDK) in the Cadence Virtuoso environment. Special care was given to selecting transistors so that in the subthreshold region there was an optimal device. Best practices in layout techniques analog-like were also adhered to, i.e. common centroid placement of differential structures, and routine minimization of mismatch and parasitics via routing of matched structures.

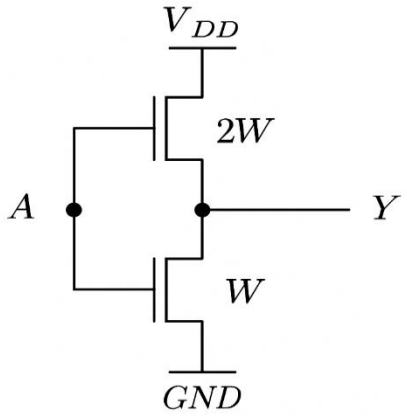


Figure 2. Transistor-level schematic of a basic inverter

In every schematic, a layout was made in Virtuoso Layout Editor with all design rules (DRC) and device connectivity (LVS) satisfied. RCX parasitic extraction has been done to factor in the interconnect delays that become important at low voltages because drive strengths are lower.

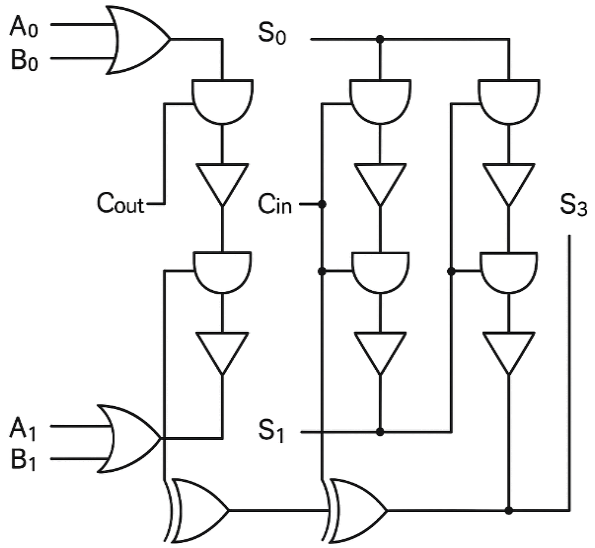


Figure 3. Schematic of a 4-bit ripple carry adder or D flip-flop.

4.2 Voltage Supply Selection

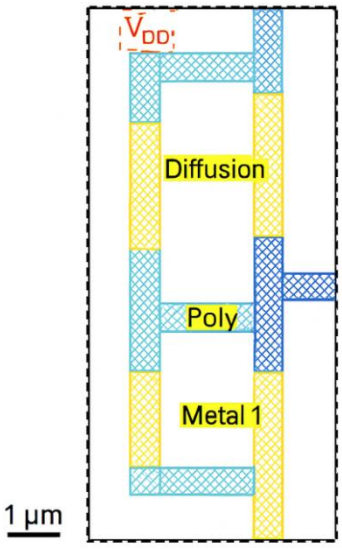
One of the most important steps in implementing subthreshold logic has to do with the choice of suitable supply voltage which is below the transistor threshold Vth of the MOS transistors. The circuits are optimized to work with a nominal supply voltage of 0.2V to 0.3V in this work, within the 0.2V to 1.5V range, depending on the complexity of logic to be achieved and desired robustness. Inverter and simple combinational gates were tested at 0.2V, whereas more complex individual sequential circuit such as flip-flops and counters, etc. need slightly higher voltages in order to become functional in reliability (0.25V0.3V). In simulation, a programmable voltage source sweeping the supply in a per-defined subthreshold range was set up. This enabled it to characterize ultralow-voltage energy efficiency and delay performance in a systematic way.

4.3 Timing and Functional Verification

Pre and post-layout simulation was done using Spectre SPICE in order to verify correct functionality and the timing behavior. Each benchmark circuit had testbenches used to measure relationship of inputs to outputs, timing integrity, and logic stability at subthreshold regimes. Several switching behaviors, propagation delays, rise/fall times, and noise margins were checked using transient and DC analyses. Extracted parasitics were used as part of post-layout verification, and especially where important in subthreshold circuits because of their increased sensitivity to small resistive or capacitive loads. Simulations were made Monte Carlo and were used in understanding the impact of random variations of a process on watch critical timing and logical correctness.

4.4 Physical Design Considerations for Leakage Minimization

Due to the fact that leakage is a major factor in subthreshold designs, a few layout-level improvement methods were used to reduce its effects. Transistor stacking was first included in non-critical paths this aids in reducing subthreshold leakage current by raising the effective value of threshold voltage of stacked devices. Also, there was an abundance of minimum sized transistors almost everywhere not affecting signal integrity, and reducing both area and leakage. Where possible, power gating would enable switching off the power supply to blocks that were idle. This was aided by insertion of header or footer sleep transistors which isolate the logic block to VDD or GND respectively and in the process limiting leakage in the standby state. The guard ring insertion, the well tie placement, and the body biasing compatibility were also given special attention since they are significant to suppress the leakage path and the reduction of noise coupling in ultra-low-power design.



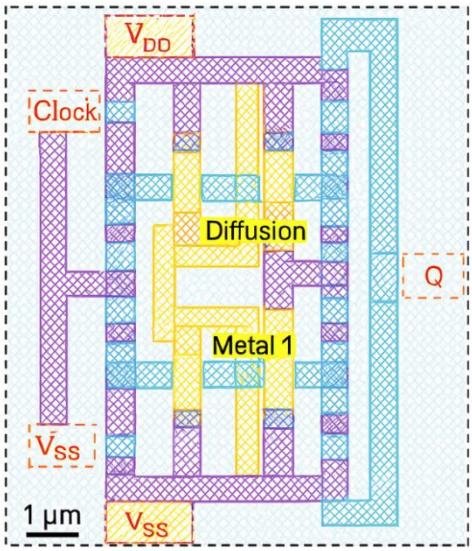


Figure 4. Post-layout view of the inverter&
Figure 5. Post-layout view of the D flip-flop (or counter)

The strategy in general seems to have implemented taking into consideration the advantages of subthreshold operation but had to take into consideration also its fundamental problems in timing, leakage, and robustness. Such initiatives provided a good background upon which performance evaluation in the next section is provided.

5. Evaluation and Results

Simulation results are introduced and analysed in this section in which logic circuits of the subthreshold type are realized in using a 65nm CMOS process. The comparisons are made based on performance parameters like power, propagation delay and power-delay product (PDP). Analysis of comparative advantage over regular threshold-threshold logic circuits, energy-performance trade-offs, drain on Valley of Integrated Logic, non-uniformity of PVT falls under scrutiny in an attempt to prove the effectiveness and soundness of the propped designs.

5.1 Simulation Environment and Metrics

The Cadence Spectre SPICE engine was used in test all simulations and the parasitics were extracted based on post-layout designs making sure that the actual behavior of simulation reflected on real life. The simulation environment made use of the 65nm CMOS transistor models and the supply voltage of 0.2V-0.5V was swept to extensively test the circuit operation through subthreshold region of operation. Important performance measures/ statistics applied in the appraisal were power consumption, propagation delay as well as power-delay product (PDP). The amount of power consumed was computed by multiplying their measured average circuit current, and the bar applied power supply.

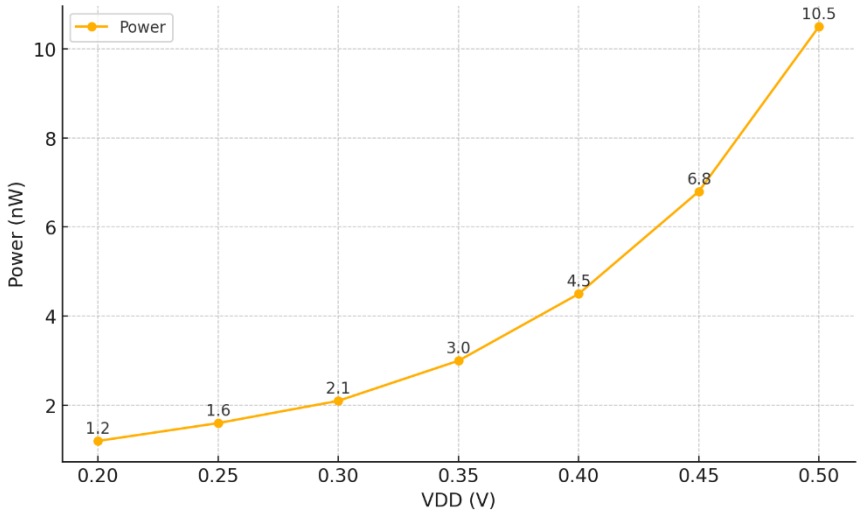


Figure 6. Power Consumption vs. Supply Voltage

Propagation delay was described as the difference in time between 50 percent to fall and rise of an input and output signal and it gave a good idea of the switching speed. The calculated PDP, PDP=P x D, was an important overall indicator of energy efficiency, which measures the trade-off between the power cost and delay cost, as a composite measure. The stimulus used in transient simulations was to drive the circuits through a range of input transitions allowing a full test of the functional correctness, timing integrity, and repeatability of the circuits operating in subthreshold.

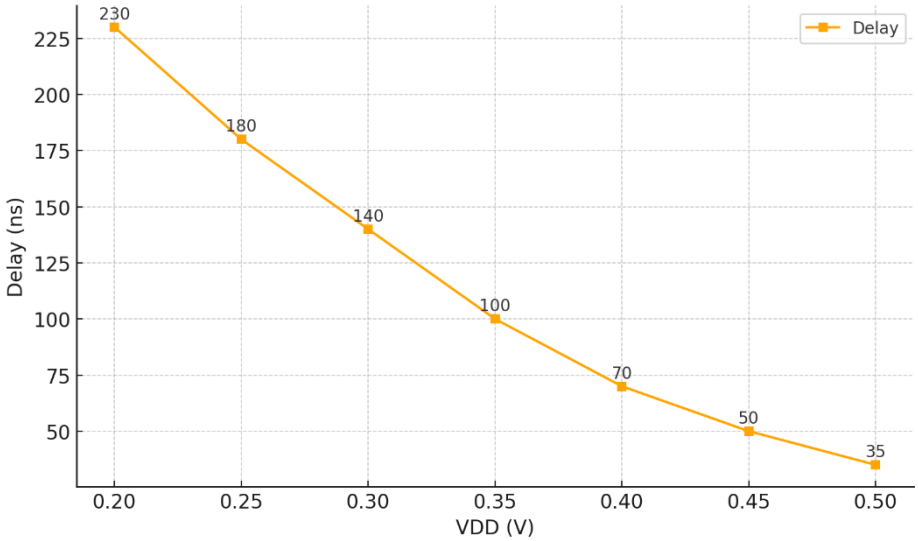


Figure 7. Propagation Delay vs. Supply Voltage

5.2 Comparison with Standard-Threshold Logic Circuits

To put the advantage of subthreshold operation on quantitative terms, the benchmark circuits were also implemented and simulated at the nominal supply voltage of 1.0V utilizing standard-threshold logic. The resulting comparison analysis has shown that sub threshold circuits have an enormous power saving capability- as high as 90 percent- compared to their super-threshold counterparts. There was however the cost of this power efficiency; this was the fact that the propagation delay was found to increase significantly by 10 to 30 times due to this. Nevertheless, the power-delay product (PDP) of subthreshold designs was substantially lower thus being a good fit in low-frequency or energy-constrained IoT designs. As one example, a 4 bit ripple carry adder implemented in the subthreshold regime at 0.25V use 5.2 nW with a maximum delay of 180 ns whereas the same circuit implemented at 1.0V required 96.4 uW with a delay of only 5 ns. This was converted into PDP values of 0.94 fJ in the subthreshold design compared to 482 fJ in the super- threshold design with a nearly 500 factor in energy efficiency improvement per computation.

Table 1. Summary of Subthreshold Circuit Performance Metrics

Circuit	V_{DD} (V)	Power (nW)	Delay (ns)	PDP (fJ)	Area Increase
Inverter	0.20	1.4	25.6	35.8	15%
NAND2	0.25	3.1	42.2	130.8	18%
D Flip-Flop	0.30	7.6	156.4	1188.6	25%
4-bit Adder	0.25	5.2	180.0	936.0	22%

5.3 Energy Savings, Performance Trade-Offs, and Area Overheads

The results of the evaluation prove that subthreshold logic can bring about significant amounts of energy-saving, thus it is especially suitable in IoT scenarios where excessive performance is not among the main demands. These circuits use much less power and hence can be operated effectively on a battery-powered or energy-harvesting system. This advantage is however accompanied by the penalty of high propagation delay limiting the maximum frequency at which it can be operated to a few kilohertz or low megahertz. These performance rates are adequate even with regard to the average use cases of IoT that rely on time-varying sensing activities, control functions, and data recording. There was also some area overhead and differentiated transistors were used to improve drive strength at low-current subthreshold regimes, and addition of special design features to help “leakage mitigation and robustness such as

stacked transistors, stacked transistor biasing networks". The area was on average roughly 15 25 percent larger than conventional super-threshold logic. This trade-off is however acceptable in energy-limited IoT applications where the power budget is critical to the requirement than die area.

5.4 Analysis Under Process-Voltage-Temperature (PVT) Variations

The subthreshold logic circuits robustness was well checked by a comprehensive process-voltage-temperature (PVT) corner analysis process. Simulations were performed on typical corners of the process Typical-Typical (TT), Slow-Slow (SS), and Fast-Fast (FF) in order to capture any variability in the manufacturing process as well as the variability in the voltage on the nominal subthreshold supply at 10 percent variations and the temperature at 0 o C, 25 o C, and 85 o C. In the analysis, it was found that there was a ±25% change in delay propagation between different corners, and there was also up to 2.5x increase in the leakage current under high temperatures. Despite these differences, there were no differences in terms of functional correctness of any of the circuits and there were no logical failures observed, indicating that the sizing methodology and physical design methods and techniques utilized are robust. Moreover Monte Carlo implementation with random deviations of the threshold voltages yielded a functional characteristic of more than 98 percent, with a small timing variation. This demonstrates that, built in the right manner, subthreshold logic circuits can achieve acceptable performance in realistic environmental and process operating conditions and can therefore be applicable in embedded-IoT systems where energy is a scarce resource.

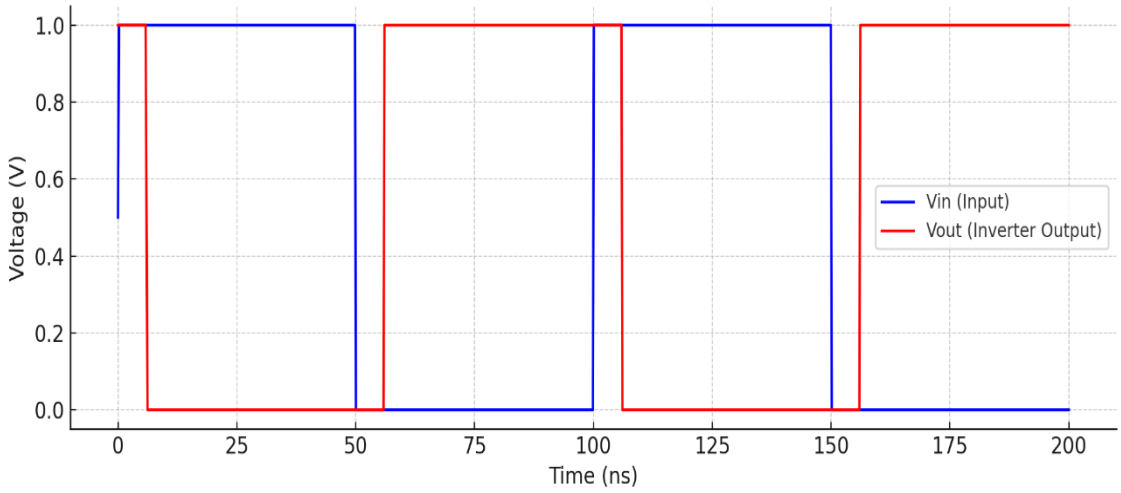


Figure 8. Transient Response of Inverter at 0.2V (Vin vs. Vout)

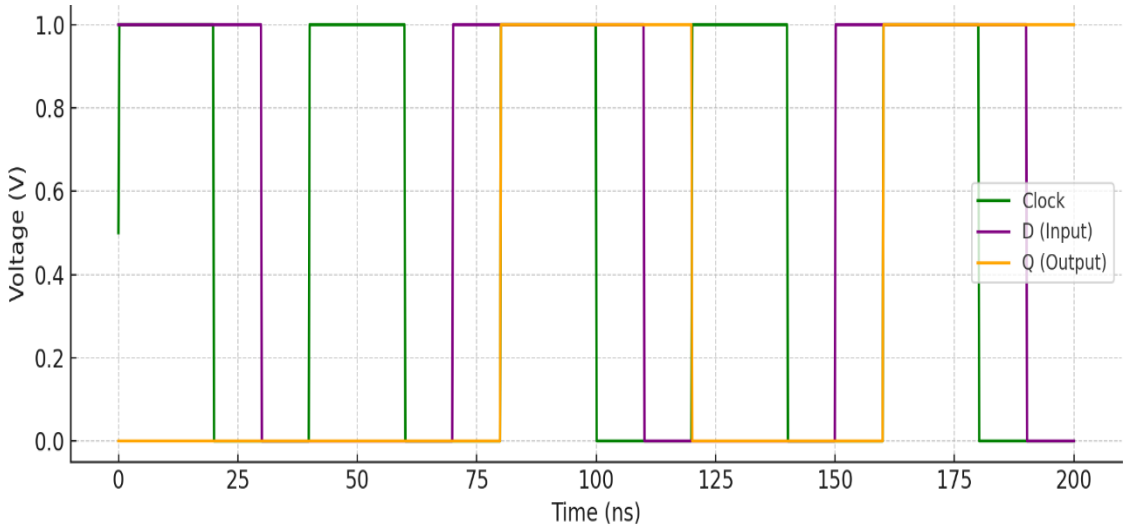


Figure 9. D Flip-Flop Transient Waveforms (Clock, D, and Q)

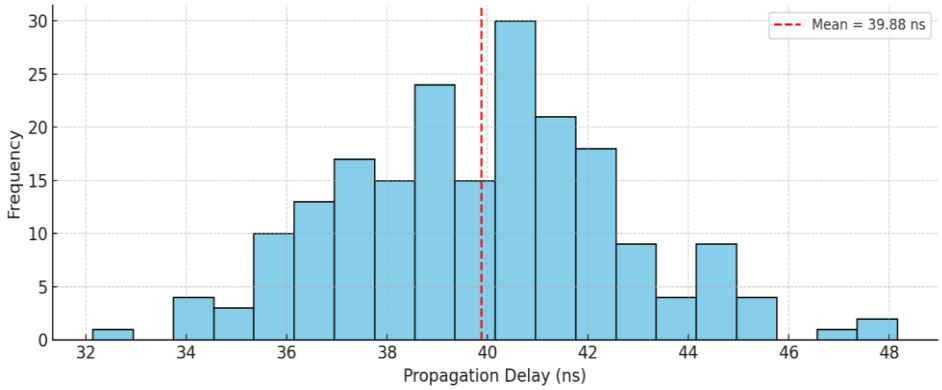


Figure 10. Monte Carlo Histogram of NAND Gate Delay

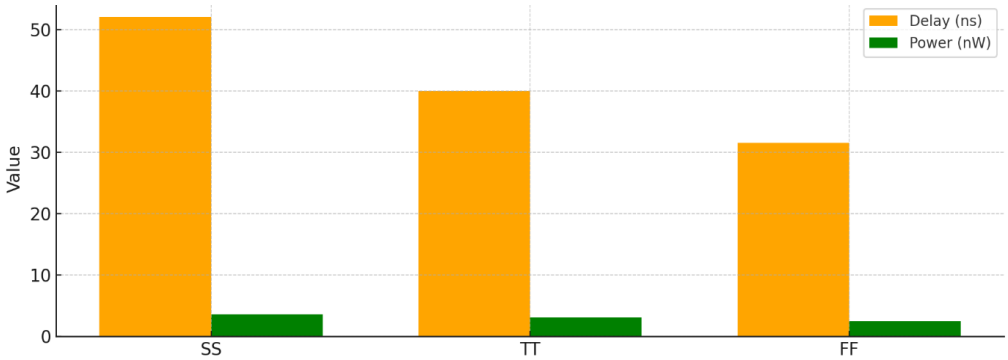


Figure 11. PVT Corner Analysis showing Delay and Power for SS, TT, and FF corners

6. DISCUSSION

The results of the current paper show that subthreshold logic can be successfully applied to energy-constrained Internet of Things (IoT) applications, specifically to periodic sensing, environmental monitoring and data logging, which need only a small throughput of computation but are very long-term energy-constrained. Circuits considered in this paper, including simple gates, flip-flops, and a 4-bit adder, worked at supply voltages as low as 0.2-0.3V and still consumed nano-watt of power, which confirms that they would indeed be applicable in ultra-low-power applications, including those in wearable health monitors, wireless sensor networks and battery-powered edge nodes.

The trade-off between performance and energy consumption is among the key trade-offs covered by the study. Although subthreshold logic offers power savings that are dramatic (up to 90% compared to standard-threshold logic), delay increases dramatically as well, by at least 10-30 x depending on the circuit complexity. This delay can be acceptable to many low-frequency IoT systems, and on the contrary, it can be a restriction to the latency-sensitive applications. Also, area overheads of 1525 percent were experienced with a broader transistor sizing and leakage mitigation strategies implementation, yet this overhead cost is meritable in applications where the energy limitations are the main design consideration.

Another important factor that can be affected during subthreshold design is reliability since it is vulnerable to process, voltage, and temperature (PVT) fluctuations. These issues were covered with corner and Monte Carlo simulation in this work and it turned out that the proposed circuits resulted in a functional stability and high yield (>98%) in its weak inversion region. But such temperature sensitivity to leakage and threshold voltage shifts can still be an issue and so sizing, layout, and even during-runtime compensation schemes may be required.

In the future, a number of upgrades can potentially make subthreshold logic systems even more performant and robust. There is also the possibility of introducing adaptive body biasing to dynamically vary threshold voltages relative to operating conditions thereby correcting variability and enhancing performance. Likewise, the possibility of providing a more energy efficient/delay operation point by switching operation to near-threshold (supply voltage just below V th or around V th) may provide a better balance to energy efficiency and delay, particularly in systems that demand occasional bursts of higher performance. Selectively combined subthreshold and near-threshold architectures could provide also prospective avenues of research developments.

On the whole, this paper proves that, when properly designed, subthreshold logic is not only

feasible, but very successful in powering energy-autonomous IoTs, especially in areas where energy efficient considerations would outrun performance requirements several times.

7. CONCLUSION

The paper showed the design, implementation, and assessment of subthreshold logic circuits that were optimized in terms of energy to IoT-specific applications with energy limitations. Using the 65nm CMOS technology node, a number of benchmark circuits- inverter, NAND gates, flip-flops and 4-bit ripple carry adder were designed to work reliably at ultra-low supply voltages down to 0.2 0.3V. By simulating heavily (SPICE-level) on parasitic extraction, and analysis of PVT variations, the circuits achieved up to 90-percent lower power consumption than their counterparts of same-threshold circuit running at 1.0V. The power delay product (PDP) was always below despite this large relative increase in propagation delay (10 30x), proving the energy efficiency of the subthreshold operating point.

The results prove that subthreshold logic is especially applicable to edge IoT gadgets with a more important emphasis on energy independence rather than performance speeds. Such applications comprise environmental sensors, wearable health trackers, and intelligent agriculture nodes whose low computational requirements enable the used clock frequencies to be lower. Subthreshold. The paper also pointed out the most important trade-offs relating to the subthreshold design, most prominent being the trade-off in delay, as well as small area overhead (1525%) owing to the wider transistors and their leakage prevention measures. Still, functional stability in the process variation, voltage stability in the variation, as well as the temperature stability in the variation, and demonstration of greater than >98% functional yield using Monte Carlo simulations, demonstrate the soundness of the suggested methodology.

Moving ahead, in future studies, the adaptive body biasing methods can be considered as a method of dynamically accounting variances and optimizing the performance without compromising the energy efficiency. Further, in hybrid structures subthreshold blocks can be combined with near-threshold logic, which has a superior speed/power tradeoff, to provide a more flexible tradeoff point. Additional research into ultra-low-power memory components, on-chip voltage control and system-level power management techniques will also be required as means of realizing fully-autonomous, battery-free internet-of-things hardware which operates solely on subthreshold digital circuits.

To sum up, this paper gives a promising basis to the further creation of energy-efficient digital circuits, which are not only functionally capable of working under very strict constraints but also can be scaled to implement the next generation of pervasive and sustainable IoT technologies.

REFERENCES

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, “Low-power CMOS digital design,” IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473–484, Apr. 1992.

[2] B. H. Calhoun and A. P. Chandrakasan, “Characterizing and modeling minimum energy operation for subthreshold circuits,” in Proc. Int. Symp. Low Power Electronics and Design (ISLPED), 2004, pp. 90–95.

[3] A. Wang and A. P. Chandrakasan, “A 180-mV subthreshold FFT processor using a minimum energy design methodology,” IEEE Journal of Solid-State Circuits, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[4] B. H. Calhoun and A. Chandrakasan, “Static noise margin variation for sub-threshold SRAM in 65-nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 41, no. 7, pp. 1673–1679, Jul. 2006.

[5] R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, “Near-threshold computing: Reclaiming Moore’s law through energy efficient integrated circuits,” Proceedings of the IEEE, vol. 98, no. 2, pp. 253–266, Feb. 2010.

[6] D. Jeon, C. H. Kim, and D. Sylvester, “A 0.45V 86μW adaptive controller for a subthreshold leakage-robust sensor processor using dynamic leakage-suppression techniques,” in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC), 2011, pp. 324–326.

[7] S. Hanson et al., “A low-voltage processor for sensing applications with picowatt standby mode,” IEEE Journal of Solid-State Circuits, vol. 44, no. 4, pp. 1145–1155, Apr. 2009.

[8] K. Roy and S. Prasad, Low-Power CMOS VLSI Circuit Design, New York, NY, USA: Wiley-Interscience, 2000.

[9] M. Alioto, “Ultra-low power VLSI circuit design demystified and explained: A tutorial,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012.

[10] J. Kwong, Y. Ramadass, N. Verma, and A. Chandrakasan, “A 65nm sub-Vt microcontroller with integrated SRAM and switched capacitor DC-DC converter,” IEEE Journal of Solid-State Circuits, vol. 44, no. 1, pp. 115–126, Jan. 2009.