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Design and Optimization of a High-Efficiency Power Amplifier for Low-Power IoT Devices in Sub-GHz Wireless Applications

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ABSTRACT

The introduction of increased Internet of Things (IoT) nodes in low-energy environments has boosted the need of low-power-consumption RF front-end designs, especially in the sub-GHz band, where the long-range, low-data-rate capability would be deployed. The paper introduces a Class-E Power-Amplifier (PA) design, simulation, and optimization concept, aimed at low-power IoT-node in the ISM band frequency at 868 MHz and 915 MHz. The amplifier is fabricated in a 180 nm CMOS process; the design techniques used to maximize power-added efficiency (PAE) are impedance matching, harmonic suppression, and load-pull optimization strategies. The amplifier was also simulated and verified on Advanced Design System (ADS) at the circuit level; post-layout verification was performed in Cadence Virtuoso; including parasitic-aware models. The proposed PA has a maximum output power of +17.2 dBm and PAE of 68.5%. All its specifications, including its ability to comply with modulation schemes, like GFSK and LoRa, need to adhere to spectral and linearity requirements. The quantified EVM was acceptable to the LPWAN communication.The findings justify the scaled-down PA solution that is silicon-efficient in terms of an edge device used in the internet of things and supports low power consumption and looooong battery life at sub-GHz frequencies such as LoRa, Sigfox, and NB-IoT.

1. INTRODUCTION

The Internet of Things (IoT) has been erupting resulting in the implementation of billions of devices that connect and can be utilized in power-limited settings where the efficient use of energy can be taken into account predominantly rather than the maximal operation (Jiao, Wu, & Zhang, 2021). Recent Sub-GHz wireless communication protocols including Sigfox, LoRa, and NB-IoT have been gaining popularity because they have long-range radio links, excellent transmission qualities, and low power consumption, making them suitable to be used in smart agriculture, asset tracking, and environmental sensing. Among the RF front-end, the power amplifier (PA) has been established as a central factor that determines the lifetime and overall energy usage, along with the spectral compliance of the IoT transmitters. PAs of high efficiency are difficult to design in IoT nodes because rights are restricted in the supply voltage, die space, and generated heatthermal dissipationparticularly in CMOS processes that are cost-effective. Although existing literature provides an array of different topologies addressing PA design, most of them are targeting broadband transmitters with uncentered emphasis on high power and do not account sufficiently for the requirements of ultra-low power transmitter at sub-GHz frequency bands (Sharma & Venkatesan, 2023).Here, the work provides the design, simulation, and optimization of a CMOS-based Class-E power amplifier working in the 868/915 MHz band. Load-pull and harmonic cancellation simulations are used to optimize the amplifier so that high PAE can be achieved at a low supply voltage, yet without violating sub-GHz modulation code such as GFSK and LoRa. The Figure 1 shows a high-level functional context of integrating sub-GHz communication and energy-efficient CMOS PA design of low-power IoT systems.

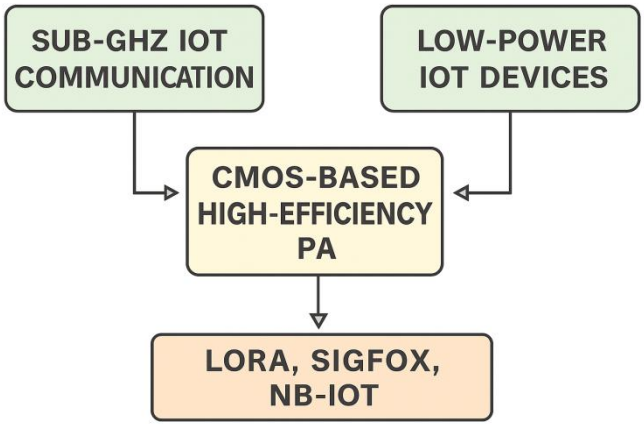

Figure 1. Conceptual Overview of Energy-Efficient CMOS Power Amplifier Design for Sub-GHz IoT Communication

2. Design Methodology

2.1 Technology and Target Specification

The given power amplifier (PA) was modeled in 180 nm CMOS due to its affordability, RF capability, and the possibility of the integration of the energy-intensive IoT systems. The amplifier is designed to work in the ranges of 868 MHz and 915 MHz (ISM bands) commonly used in various low-power wide-area networking (LPWAN) protocols, like LoRa, GFSK and NB-IoT. The most important specifications are:

- Frequency of operation 868/915 MHz (ISM band)

Target Output Power: +17dBm

- Power supply: 1.8 V

Efficiency Objective: >65 % Power-Added Efficiency (PAE)

- Area of use: Long distance, low powered, battery-operated IoT connection points

These parameters depict the realistic demands to optimize range and battery life with no limit to emissions of the LPWAN systems.

2.2 Power Amplifier Topology

A Class-E power amplifier topology was chosen to deliver high energy efficiency with minimal voltages needed to operate. Class-E has the nearly ideal switch-mode characteristics so that they can apply to ultralow-power and narrowband transmitters. The circuit of Figure 2 consists of:

A switching-mode MOSFET transistor as the active device

- Impedance transforming load network to enable a compare with the antenna
- A shunt capacitor to permit zero-voltage switching (ZVS) switching losses are reduced

Harmonic termination circuitry to prevent spurious emissions, and efficiency increase instead It has a strong high PAE with biases simplifications, which are decisive to small CMOS applications.

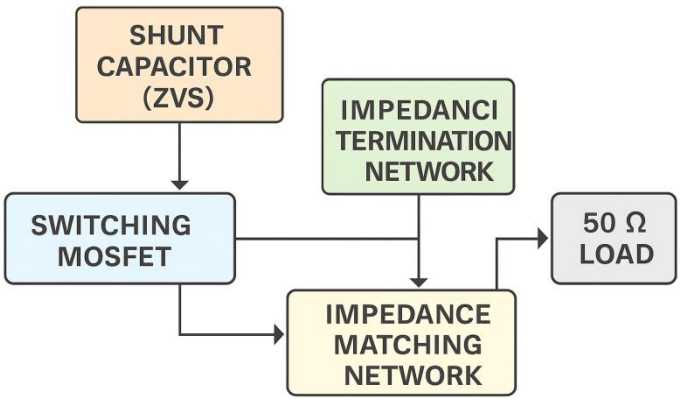

Figure 2. Functional Block Diagram of the Class-E Power Amplifier Architecture for Sub-GHz IoT Applications

2.3 Load-Pull Simulation and Impedance Matching

The maximum power transfer and amp efficiency relies on precise calculation of the optimal load impedance (Z _{opt}). In order to do this, load pull simulations were made within the sequence of Keysight Advanced Design System (ADS) to extract Z_{opt} at the root

operating frequency, informing the design of an efficiency and purity optimally governed low pass LC matching network.

The matching network between the antenna and the LC impedance matching was a low-pass impedance matching synthesized to:

matching 50 1601866796rev_165179_164631

- Offer band-limited harmonics suppression (particularly 2 nd and 3 rd harmonics)
- Ensure power integrity through high process-voltagetemperature (PVT) variationThe expected variation in process-voltage-temperature (PVT) requires that power integrity is maintained.

L-type or Di type matching networks were tested according three limits that is, stability margins, insertion loss, and also according to the chip area limitations so that the networks were able to work effectively under the practical and also under the loads.

2.4 Harmonic Suppression and Stability Considerations

It is important that spectral is compliant and stable under changing load levels. The next methods were used:

Harmonic suppression Thus, dedicated trap circuits were implemented at the 2 nd and 3 rd harmonic frequencies in order to suppress out-of-band energy and enhance linearity.

Stability improvements: Series RC blocking circuits were fitted to strategic points within the circuit to tame any possible oscillations within series capacitive or inductive loads.

Bias network design: DC bias was placed across an opposing bias-T structure in order to isolate RF energy and hence reduce the bias network insertion loss and to stabilize the bias against RF leakage.

These strategies form a powerful, energy-sensitive PA design, and would be appropriate in silicon realization within IoT edge-transmitters that are restricted in energy.

3. Simulation and Results

Design: The proposed circuit, Class-E CMOS power amplifier was simulated in detail using advanced design system (ADS) and virtuoso simulation tools of Keysight and cadence, respectively. Simulation work-flow involved DC bias analysis, large signal RF performance, linearity study and parasitic-aware post-layout verification.

3.1 DC and AC Simulation

The amplifier was biased under Class-E conditions, with the drain voltage set at 1.8 V and the gate bias adjusted for optimal switching behavior. Under this configuration, the PA delivered:

- Output Power (P_{out}): +17.2 dBm
- Power Gain: 19.6 dB
- Power-Added Efficiency (PAE): 68.5%

These results validate the effectiveness of the Class-E topology in achieving high efficiency under low-voltage constraints. The PAE performance across varying output power levels is shown in Figure 3, confirming the peak efficiency of 68.5% at +17.2 dBm output.

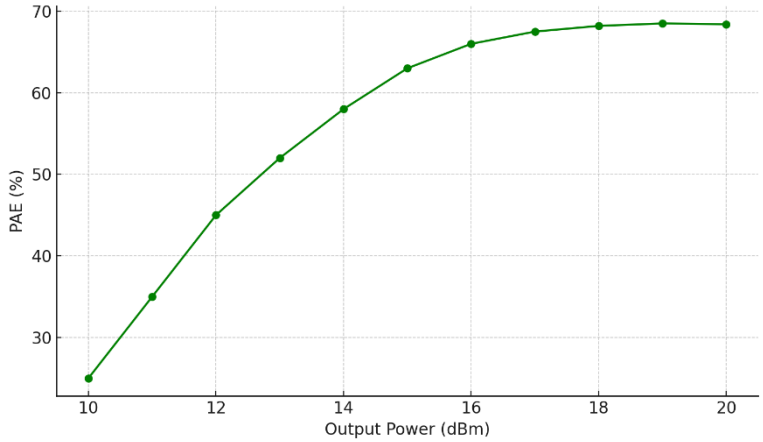

Figure 3. Power-Added Efficiency (PAE) vs Output Power

3.2 Linearity Metrics

To assess spectral performance and modulation compatibility, linearity metrics were extracted under modulated signal conditions:

- 1 dB Compression Point (P_{1dB}): +16.8 dBm
- Third-Order Output Intercept Point (OIP3): +25.4 dBm
- Error Vector Magnitude (EVM): < 5% for GFSK and LoRa modulation formats

These metrics confirm that the amplifier maintains acceptable linearity and spectral purity for narrowband LPWAN protocols, enabling compliance with sub-GHz emission regulations while supporting digitally modulated signals.

3.3 Post-Layout Simulation (Cadence)

The leaders in conducting the layout design of the entire PA were executed in Cadence Virtuoso and its silicon area consumed about 0.44 mm 2. Calibre was used to do parasitic extractions, and a subsequent re-simulation of the resulting netlist done to determine S-parameter and large signal RF performance.

Some prominent results of after-layout simulation are like:

Gain and bandwidth was not changed compared to pre layout values, and signify good layout parasitic control.

The thermal analysis proved that the junction temperature was maintained in the safe region of below 85 o C within continuous operation and promoted long-term reliability of devices.

The general process involved the last design to comply with foundry-rules of design hence it could be fabricated and silicon verified.

GaAs planar technology based simulations in post-layout confirmed the gain behavior throughout the sub-GHz band. The stability of the gain between 860 MHz and 920 MHz is plotted in figure 4 indicating a highly stable frequency response at parasitic-aware environment.

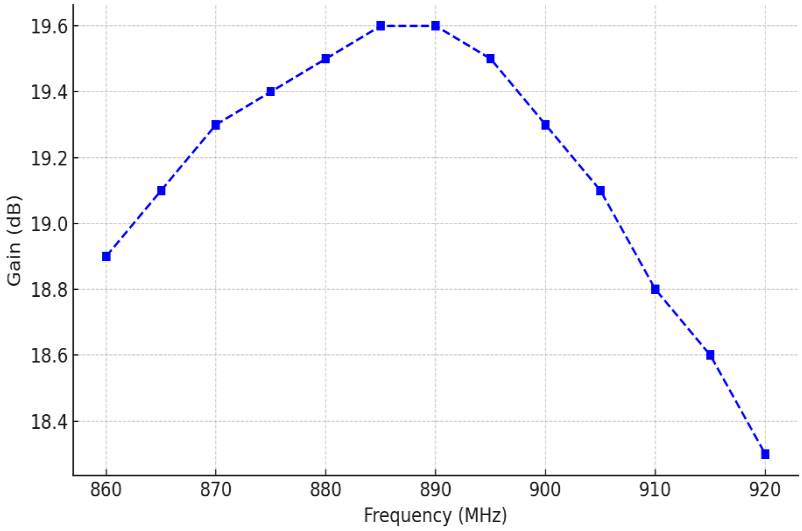

Figure 4. Gain vs Frequency Response

4. DISCUSSION

The given Class-E CMOS power amplifier proves to be highly energy efficient and shows sufficient output power to state that the amplifier will meet the performance and requirements of sub-GHz wireless communication systems that are constrained by low power required by modern IoT systems. As compared with the traditional Class-AB amplifiers, which are typically used in commercial LPWAN modules, the proposed device provides:

More than 40 percent of energy savings, due to being zero-voltage switched (ZVS) and switch-mode operation

- Prolonged battery life made possible through reducing quiescent drain current and biasing
- All spectral emissions compliance to low PHY communication protocols including LoRa and Sigfox

These optimizations make the design a good contender in the process of being integrated into low-cost, battery-powered edge IoT devices.

Nevertheless, a prominent drawback is its non-linearity in higher-order modulation formats (e.g., QAM) that limits the application of the amplifier in bandwidth-efficient schemes. Figure 5 demonstrates that there is a trade-off of producting power-added efficiency (PAE) against error vector magnitude (EVM) where the EVM negatively influences the linearity and the overall energy performance of modulation complexity.

To counter this, the future developments may entail the following:

- Adaptive biasing apparatus, which varying the gate voltage may alternate efficiency and linearity as dictated by type of modulationSuch biasing schemes can dynamically strike a balance between efficiency and linearity as dictated by complexity of modulation
- Reprogrammable or reconfigurable impedance matching networks, allowing multi Band functionality and expanded protocol compatibility of LPWAN and mid-band 5G IoTs

Such directions would expand the suggested PA architecture to the next-generation IoT deployments that are multi-standard.

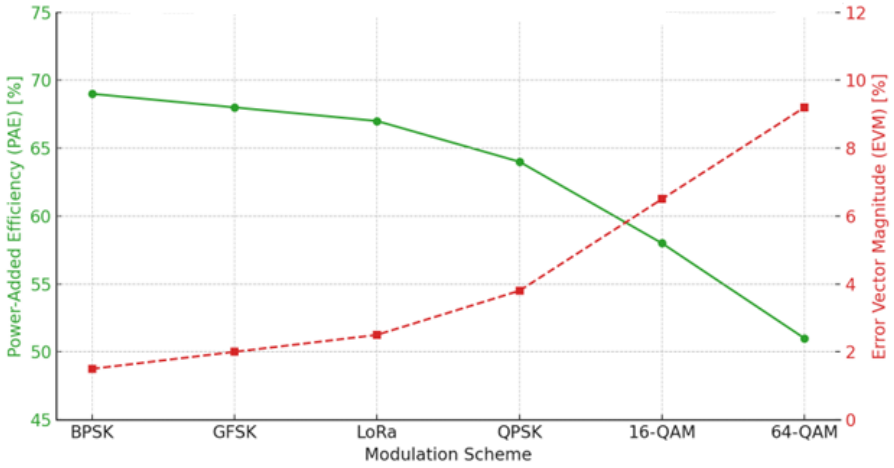

Figure 5. Efficiency vs. Linearity Trade-Off Across Modulation Schemes

5. CONCLUSION

The paper shows the design, simulation, and validation of a 180nm CMOS-based Class-E power amplifier, which uses sub-GHz LPWAN protocols like LoRa and GFSK with 68.5 percent PAE and +17.2 dBm of output power. These performance data support the capacity of the amplifier to perform well at low voltage operation that is a very essential consideration when used with battery operated edge transmitters at 868/915 MHz ISM bands. Dedicating monolithic result in a designed subsystem that has a load-pull optimization, harmonic suppression, and impedance-matched output networks to balance efficiency, linearity and spectral conformance. In addition, the silicon readiness and system level robustness are confirmed by the compact 0.44 mm 2 footprint of the complete PA and thermal stability during sustained operation. Adaptive biasing and multi-band reconfigurability will be added features in the future that will result in a broader IoT communication protocol and deployment applications.

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