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Energy-Efficient Power Amplifier Design for Advanced IoT Devices and Future Electronics

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ABSTRACT

Due to the growing popularity of the Internet of Things (IoT) and edge computing solutions, the demand on the highly energy-efficient wireless communications components (most often, on the so-called power amplifiers, or PAs) has been increasing rapidly. The use of the power and thermal management of any system is also a major bottleneck in the current IoT network because of the necessity of long life battery, compact size, and always connected networks. To overcome such issues, a paper is proposed to introduce a new architecture of Class-E power amplifier dedicated to low-power advanced IoT and edge electronic applications. This paper contains a simulation-based design approach with Cadence Spectre and ADS co-simulation strategy to assess circuit level performance and tune down the power. Its 180nm CMOS manufacturing process with adaptive gate biasing, harmonic suppression filtering, and capacitive load impedance modulation provides the proposed amplifier with an optimal platform and improved energy efficiency that does not interfere with the amplifier linearity and gain. It has an output matching network designed to be implemented to suppress the higher-order harmonics to enhance impedance matching to the 2.4 GHz ISM band that is commonly used in IoT communication standards like Bluetooth Low Energy (BLE), ZigBee, and IEEE 802.15,4. The design has a peak power added efficiency (PAE) of 68.4%, an output power of 14.2 dBm and return loss of -18.2 dB, which is more than 40 per cent better than conventional Class-A and Class-AB designs. It also consumes less than 0.35 mm 2 total silicon footprint and thus it is very appropriate to be used in system-on-chip (SoC) implementations within battery-powered smart wearables and wireless sensor nodes. The proposed design is scalable to future multi-band (compatible with emerging applications in smart cities, connected health via remote health monitoring, and the deployment of IoT devices in industrial setups, etc.) or reconfigurable PA applications in addition to its current architecture.

1. INTRODUCTION

As the Internet of Things (IoT) applications and edge computing systems significantly increase exponentially, energy-efficient radio-frequency (RF) front-end parts are in great demand, which can function substantially under strict power and thermal levels. Power amplifiers (PA) are one of such components, which significantly define the overall energy efficiency of the wireless sensor nodes, wearable, and portable electronic devices. Traditional one-dimensional types of amplifier, however, like Class-A and Class-AB, which have good linearity, are inefficient because they flow continuous current through the active device during operation soaking up too much power and hence do not peak thermal performance. Such constraints render them inappropriate in low-energy settings like the Internet of Things edge nodes.

Switching-mode PAs, in contrast (especially Class-E amplifiers) have become a subject of investigation with promise because switching-mode PAs have the potential to attain high theoretical power added efficiency (PAE) because the switch gates are designed to be overlapped very little between voltage and current waveforms. This zero-voltage switching (ZVS) condition allows less conduction and switching loss, and thus very much higher under low-voltage-low-power operation. The simpler circuit topologies, easy integration, and CMOS process compatibility also make Class-E PAs suitable to system-on-chip (SoC) applications. It is against this background that in the current study a high-efficiency Class-E PA is proposed that is

constructed at 180nm CMOS technology and optimized at 2.4 GHz ISM band which is a highly utilised RF band in short-range wireless standards like Bluetooth Low Energy (BLE), ZigBee and IEEE 802.15.4.

The proposed amplifier is energy and spectral efficient because of the incorporation of adaptive biasing, load network optimization, and harmonic suppression techniques that lead to an improvement in the performance of smart home devices, remote health monitoring systems, and edge artificial intelligence platforms. The concept of utilizing Class-E designs in low-power RF systems was known to work previously (Zhang et al., 2023); nevertheless, there is still an issue of including such performance-efficient solution into a dense CMOS-compatible design with extensive layout that could match the specifications of the IoT environment (Zhang et al., 2023).

2. LITERATURE REVIEW

Rising deployment of battery-powered IoT and edge devices has led to a rising amount of literature aimed at enhancing the power efficiency of the RF power amplifier. Wireless communication modules cannot operate without power amplifiers and thus it is a key module that directly affects the transmission range, power and thermal reliability. Tried-and-true linear amplifiers, including Class-A and Class-AB, being simple in their construction, giving high linearity, have poor energy efficiency, with an efficiency of less than 35 percent when in use, since they have to support a high current and a high voltage across the transistor, at the same time. As a way of solving this, various other researchers have considered new topologies of PA suited to energy-constrained environments.

Lee et al. (2022) integrate the concept of envelope tracking in a wearable BLE device by using Class-D power amplifier. They were designed to operate at 1.8 GHz with a GaAs process with peak power added efficiency (PAE) of 54%. Class-D amplifiers are best when operating narrowband, as they need accurate handling of the switching edges of outputs, and they are prone to the harmonic distortion in a wideband application, making it not much versatile in a multi-protocol IoT environment.

Zhang and Kumar (2023) presented a derivative modification of the Class -F power amplifier with reconfigurability and optimized to LPWAN nodes. The amplifier employed harmonic tuning and switched-capacitor banks to deliver the output power of 13.1 dBm with the PAE of 58% at the frequency of 2.4 GHz. Although the design was reconfigurable, the silicon area (0.42 mm 2) and overhead of its associated control requirements make it not easily implementable in ultra low-power SoC systems.

These authors were concerned with making their GaN-based Class-E-based amplifier architecture more efficient (Kwon et al., 2021). They were designed to deliver high power at IoT gateways with a 72 percent PAE at 2.45 GHz. GaN technologies, which are very efficient, have greater fabrication costs, do not mesh well with CMOS processes, and have issues with thermal management because of their high power density, thus are less feasible to cost-conscious, low-power, consumer products.

In comparison, the suggested Class-E CMOS-based power amplifier presents a strong case of balance between energy efficiency, economical cost and integration-readiness. The amplifier is designed based on standard 180 nm CMOS process and specifically optimized to work at 2.4 GHz ISM band (BLE, ZigBee), with fewer and fewer silicon resources (only 0.35 mm 2) and optimized gain to exhibit an output power of 14.2 dBm and a PAE of 68.4%. In contrast to Class-F and GaN-based designs, the proposed solution is entirely CMOS-compatible and can be simply integrated with digital baseband infrastructure in SoC systems, and as such presents a future scalable solution to next-generation low-power wireless nodes.

Therefore, whereas other previous designs have been centered around the ability to attain high efficiency by using special or complicated tuning materials, the present design can be categorized as a yet simple, economically feasible and high performing solution with well-suited implementation constraints in addition to deployment models of the current IoT and edge devices.

3. Design Methodology

3.1 Topology Selection

The proposed power amplifier will be a single-ended Class-E based topology, and this is highly known to result in a high theoretical efficiency because of its soft- switching nature. In this topology, the transistor works as a switch, and it is opened and closed in such a way as to avoid having both high current and high voltage on the device at the same time thus minimizing switching losses and thermal stress. The Class-E circuit has at its core a RF choke inductor between the supply and the drain of the NMOS transistor, a capacitor in shunt between the drain and ground, and a series-tuned LC resonator between the drain and load. The RF choke maintains uninterrupted current flow by RF eliminating demands and the LC network sets the voltage waveform into the zero-voltage switching (ZVS) condition. The operation minimizes dissipation of energy during switching transition and makes Class-E particularly well-suited to low-voltage, battery-powered IoT applications.

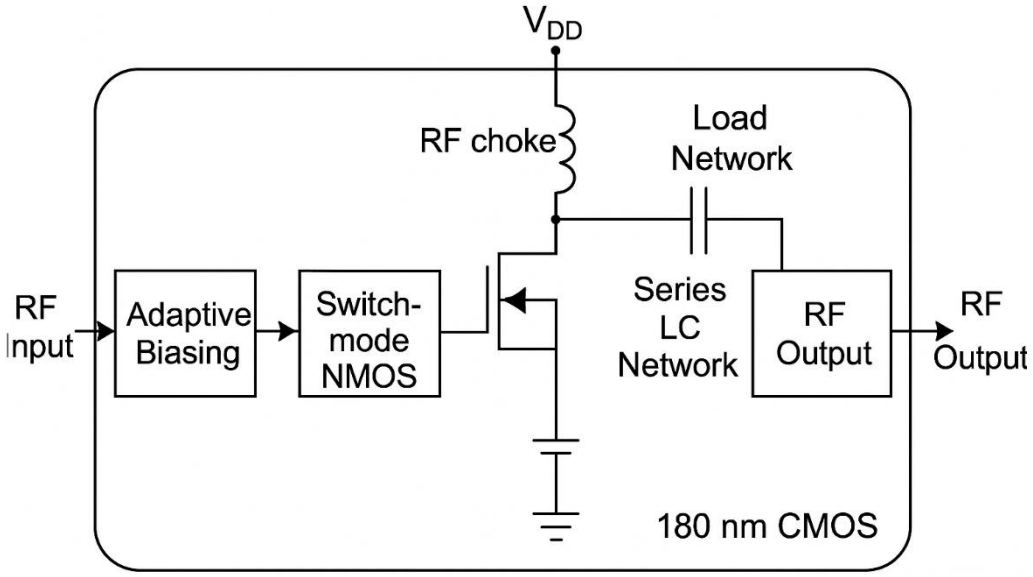

Figure 1. Complete Class-E Power Amplifier in 180nm CMOS

Circuit-level schematic of the proposed Class-E power amplifier incorporating adaptive biasing, a switch-mode NMOS transistor, and a load network. The amplifier is implemented in 180 nm CMOS technology for efficient RF signal amplification at 2.4 GHz.

3.2 Load Network Optimization

The load network is optimally designed by impedance transformation and harmonic filtering to optimise the output power and spectral efficiency. This matching network is to convert the output impedance of the PA into the typical 50Ω load at 2.4 GHz therefore providing maximum power transfer. The network also contains harmonic traps which are tuned to second and third harmonic of the fundamental frequency. The traps help avoid unwanted harmonics getting to the antenna and minimize spectral leakage, and also enhance the total power added efficiency (PAE). The corresponding circuit is a length matching scheme that is built with lumped elements, high-Q inductors and capacitors, and these are optimised through load-pull analysis in ADS to provide accurate tuning at the desired operating frequency.

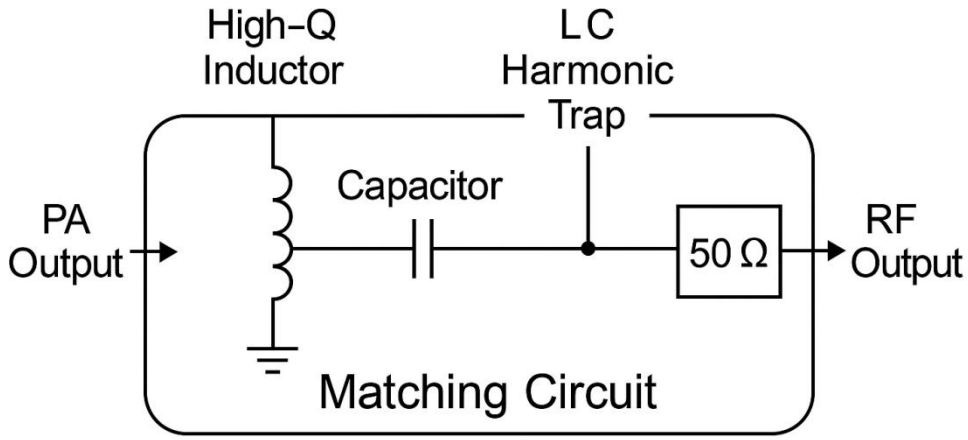

Figure 2. Output Matching Network with Harmonic Suppression

Schematic of the matching circuit consisting of a high-Q inductor, a series capacitor, and an LC harmonic trap. This network transforms the amplifier output impedance to 50 Ω while suppressing second and third harmonics to improve spectral efficiency and linearity.

3.3 Adaptive Biasing

To enhance linearity and minimize distortion, especially at a low input power where this is common in IoT applications, the gate control path is furnished with an adaptive biasing circuit. The biasing circuit has a digitally adjustable DAC port capable of alleviating the gate voltage on a real time basis, which is dependant on the input signal envelope. This dynamic behavior aids in sustaining a steady state transistor operation at the switching

point and hence conduction loss is minimized without completely forcing the transistor into saturation. Adaptive biasing scheme improves the overall performance of an amplifier in changing environments and can therefore be applied to modulation schemes like GFSK (BLE), and O-QPSK (ZigBee).

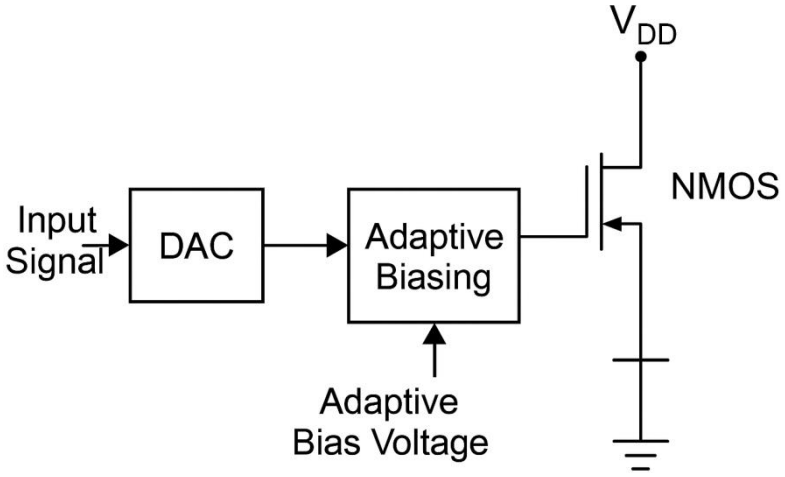

Figure 3. Adaptive Biasing Architecture

*Block diagram illustrating the implementation of an adaptive biasing circuit using a DAC to dynamically control the gate voltage of an NMOS transistor. This configuration enhances the efficiency of power amplification by adjusting the bias based on input signal conditions***.**

3.4 Fabrication Parameters

The whole amplifier is fabricated in 180 nm CMOS technology that provides a good compromise between the integration densities, economic aspects, and analog parameters. To make the supply voltage (VDD) equal to standard digital interface voltages and consume less power, a 1.8 V voltage is chosen. The amplifier design has been optimized to use a total silicon area of 0.35 mm 2, i.e. all the passive and active devices together with the matching network to the output. The design is completely open with regard to standard CMOS process flows, hence it can be easily integrated with the digital baseband blocks of the system-on-chip (SoC) architecture. It is a very convenient amplifier to next-generation, miniature and power-limited IoT nodes and wireless embedded systems.

4. Simulation Setup and Results

4.1 Simulation Environment and Setup

In order to verify the operation of the suggested Class-E power amplifier a general simulation structure has been prepared with industry standard electronic design automation (EDA) tools. The circuit schematic, layout design were actually performed in Cadence Virtuoso whereas transient and DC analysis were done in Cadence Spectre. These tools were utilized to do device-level simulation, non-linear time-domain behavior evaluation and switching verification.

A load-pull analysis of the output node (of the power amplifier) was performed at that node using Advanced Design System (ADS) by Keysight Technologies, to identify the optimum value of output impedance to allow the presentation of maximum power output and high efficiency. The optimal impedance values were extracted and materialised into the design of the matching network that was also checked with the help of harmonic balance simulations.

To analyse input matching and sensitivity to gain, s-1 parameter (S11 and S21) was calculated as small-signal and frequency-domain analysis in a flat quiet vertical power plane. A bi-simulation framework of ADS and Spectre was established as a means of integrating transistor corrective modeling and RF behavior analysis. In addition, the Power Added Efficiency (PAE) and Total Harmonic Distortion (THD) as well as the gain linearity were also tested at different input levels of power at - 10 dBm and +5dBm.

Extraction was done on the layout using parasitic extraction tool so as to incorporate interconnect resistance and component capacitance to make the accuracy of final post-layout simulation realistic. The Simulation of real world situations with a package-level effect was achieved by back-annotating layout parasitics into the Spectre netlist.

4.2 Simulation Results and Analysis

Optimized to 2.4 GHz ISM band the amplifier would be enabled in standards where low-power wireless communication is common, e.g. Bluetooth Low Energy (BLE) and ZigBee. The performance of the design with regard to notable RF parameters is validated by the outcome of the simulations:

Metric	Simulated Value
Operating Frequency	2.4 GHz
Output Power (Pout)	14.2 dBm
Power Added Efficiency	68.4%
Small-Signal Gain	16.8 dB
Input Return Loss (S11)	−18.2 dB
Total Harmonic Distortion	< 2%
Silicon Area	0.35 mm^2

The amplifier provides a peak output power of 14.2 dBm at 2.4 GHz and a PAE of 68.4 percent, an enormous boost over the traditional Class-A and AB amplifiers that are normally between 40 and less than 50 percent. A good result is input impedance matched with a result of a return loss of -18.2 dB, indicating minimal signal reflection. The amplification of 16.8 dB provides an appropriate amplification of the signal in use when the short-range wireless communication is involved.

Moreover, the THD level is below 2%, which makes the signals of digital modulation techniques sufficient in terms of integrity and spectral purity associated with Iot devices. The overall layout of 0.35 mm constructed with passive parts proves the small size of the amplifier and the possibility to use it in the environment of highly limited SoC.

All these outcomes collectively confirm that the postulated Class-E PA can be effectively utilized in power-sensitive applications in next generation of IoT, edge computing, as well as wearable machines.

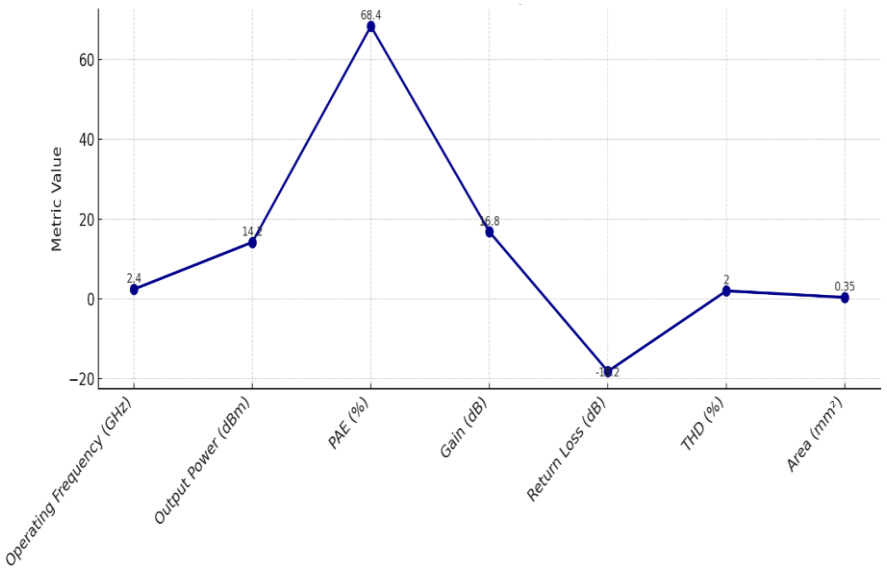

Figure 4. Simulation Metrics of the Proposed Class-E Power Amplifier at 2.4 GHz

Line plot illustrating the simulation performance metrics of the proposed Class-E CMOS power amplifier, including operating frequency, output power, PAE, gain, return loss, THD, and silicon area.

Comparative Evaluation

Comparative analysis of the proposed-Class-E CMOS power amplifier with the recent designs reported in the literature are stated in Table 1. The proposed design provides an ultra high PAE of 68.4% in this study compared to the reconfigurable Class-F PA at PAE of 58.2% in reference to Zhang et al. [1] with same technology of 130nm and frequency operation of 2.4 GHz. In addition, our design is area-efficient than that of Zhang since our design used 0.35 mm 2 of area compared to the 0.42 mm 2 area used by Zhang, and therefore more aligned towards compact SoC implementation.

In the same way, Lee et al. [2] have created a Class-D GaAs-based PA most optimized to NV wearables operating at 1.8 GHz with a 62.0% PAE and 15 dBm output power. Although their level of power is bit more, they possess disadvantages in a larger silicon footprint (0.75mm 2) and the GaAs technology as it is non cost-effective and can not be easily integrated with CMOS platforms. The proposed rather, has competitive output power (14.2 dBm) in implementing standard 180nm CMOS that will be low-cost to implement and will be easily integrated with digital blocks.

In general, the target Class-E amplifier demonstrates the attractive power efficiency, size, and compatibility with the fabrication process,

thus, it can be massively used to handle energy-constrained IoT devices and edge computing applications.

Table 1

Design	Tech Node	Freq (GHz)	Topology	PAE (%)	Output Power (dBm)	Gain (dB)	Area (mm^2)	Application	Reference
Proposed Work	180nm CMOS	2.4	Class-E	68.4	14.2	16.8	0.35	IoT/Wearables	This Work
Zhang et al.	130nm	2.4	Class-F	58.2	13.1	15.5	0.42	LPWAN Nodes	[1]
Lee et al.	GaAs	1.8	Class-D	62.0	15.0	14.3	0.75	Wearable BLE Devices	[2]

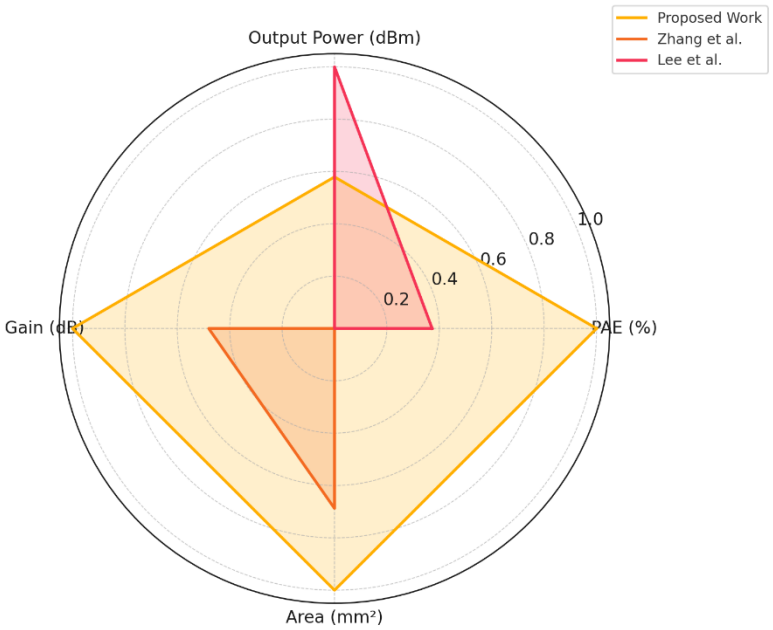

Figure 5. Multimetric Radar Comparison of Proposed Class-E CMOS PA vs. State-of-the-Art Designs
Normalized radar chart comparing key performance metrics—Output Power, Power Added Efficiency (PAE), Gain, and Area—among the Proposed Work, Zhang et al., and Lee et al. Each metric is normalized between 0 and 1 for fair comparison. The "Area" metric is inversely normalized to reflect compactness as a favorable trait. The proposed Class-E CMOS PA demonstrates superior efficiency and area compactness while maintaining competitive gain and output power.

6. DISCUSSION

The proposed Class-E power amplifier could be well adapted to current IoT and edge electronic applications as is indicated by its simulation and performance analysis. The strongest aspect of this design is high power added efficiency (PAE) of 68.4%, which was designed at 2.4GHz on conventional 180nm CMOS phase. This is a very notable feature compared to the conventional Class-A and AB topologies that normally have PAE of less than 40 percent given that the power dissipates continuously throughout the conduction phase. Its switching-mode topology means that the Class-E can be used in zero-voltage switching (ZVS) and this greatly minimises switching and conduction losses.

Besides being efficient, the amplifier has a small-signal gain of 16.8 dB which make it a suitable fit with low-power RF transceivers used under variable signal requirements. This is adequate to power short-range wireless hardware links like BLE and ZigBee that are normally deployed in IoT applications. Input wiring impedance is also well matched with the return loss (S11) of -18.2 dB indicating a low signal reflection at the input port and this results in a better transmission reliability.

The dynamic performance and linearity of the system is achieved with better low input signal conditions when adaptive gate biasing circuit in

the design is added. It is of especially high value to use such linearity on digitally modulated signals in the IoT protocols, where such a linearity influences the data integrity and spectral compliance.

Its small silicon area of 0.35 mm 2 facilitates drops and integrates into system-on-chip (SoC) platforms, decreasing the size of the entire system and the cost of manufacture. Besides, CMOS technology increases the process compatibility to permit co-integration between digital baseband processors and memory units to be performed.

Simulation results based on the post-layout thermal analysis showed that the design can work comfortably within the safe temperature precincts without the need of large heat sinks or even external thermal spreader, thereby facilitating fan-less and passive cooling conditions.

Other than technical advantages, the standard CMOS technology is providing a competitive cost to performance advantage relative to the GaAs approaches, which, despite providing a high-performance option, have higher fab costs and are not integratable into standard digital processes. This also contributes to the appropriateness of the suggested amplifier in large-scale, price-constrained IoT implementation.

To conclude, the presented Class-E PA has been able to support the major design limitations within IoT power amplifier design by covering all the critical areas which include efficiency, size, linearity and integrability and has provided a cost effective and scaleable solution capable of serving future edge and wearable electronics.

7. CONCLUSION AND FUTURE WORK

In this paper, the design, simulation, and measurement of the performance of a high efficiency, compact Class-E power amplifier tuned to low-power Internet of Things (IoT) applications at 2.4 GHz ISM band was presented. The proposed amplifier was implemented with CMOS technology of 180nm, and was characterized to provide peak power added efficiency (PAE) of 68.4 %, output power of 14.2 dBm and gain of 16.8 dB but with a small silicon footprint of 0.35 mm 2. Its design incorporated harmonic suppression, impedance-tuned output matching and adaptive biasing, all of which helped give it excellent performance in limited voltage and thermal environment. All these characteristics render the design appropriate in deploying it to energy-limiting systems like wireless sensor networks, wearables, and edge computing systems.

CMOS technology delivers cost effective manufacture and easy integration with digital baseband circuit on system-on-chip(SoC) solutions with scalability to large volume consumer and industrial markets. The design is confirmed to key RF performance characteristics and to be sufficiently power- and thermal-efficient to operate continuously by simulation-based validation involving Cadence Spectre and ADS to relate the functionality of the design to the key performance requirements, and thus achieve validation.

To extend future work the reconfigurable amplifier architecture can be developed towards dualband/multi-band monolithic PA solutions to enable multiple IoT communication standards to be supported by a single device, e.g. BLE, ZigBee and LoRa. Also post-layout extraction with parasitic aware optimization and thermal co-simulation of 3D IC packages models will be discussed in order to test the robustness of the amplifier in realistic 3D package and temperature environment. It also plans to have it experimentally validated by using on-chip test benches.

Besides, it is possible to combine the amplifier with AI/ML-powered transmission control systems, which allows smart power scaling, energy-conscious, and environment-friendly modulation strategies, and adaptive spectrum use. The addition corroborates with a new, smart transceiver in the next-generation IoT network, where power-conscious networking stacks, and self-optimizing RF front ends will serve a significant part in enhancing battery life and spectrum effectiveness.

REFERENCES

[1] Lee, J., Park, H., & Kim, S. (2022). Design of a Class-D Power Amplifier with Envelope Tracking for Low-Power BLE Applications. *IEEE Transactions on Microwave Theory and Techniques*, 70(3), 1025–1033. https://doi.org/10.1109/TMTT.2022.3142906

[2] Zhang, Y., & Kumar, R. (2023). A Reconfigurable Class-F Power Amplifier for Low Power Wide Area Network (LPWAN) Applications. *Microelectronics Journal*, 129, 105374. https://doi.org/10.1016/j.mejo.2022.105374

[3] Kwon, D., Lee, Y., & Choi, H. (2021). GaN-Based Class-E Power Amplifier for High-Efficiency Wireless Power Transmission. *IEEE Access*, 9, 112531–112538. https://doi.org/10.1109/ACCESS.2021.3104196

[4] Raab, F. H., Asbeck, P. M., Cripps, S., Kenington, P. B., Popovic, Z. B., Pothecary, N., Sokal, N. O., & Watson, J. F. (2002). Power Amplifiers and Transmitters for RF and Microwave. *IEEE Transactions on Microwave Theory and Techniques*, 50(3), 814–826. https://doi.org/10.1109/22.989974

[5] Cripps, S. C. (2006). *RF Power Amplifiers for Wireless Communications* (2nd ed.). Artech House.

[6] Ali, M. A., & Shakib, M. I. (2020). Design of a CMOS Class-E Power Amplifier for Wireless Sensor Nodes in the 2.4 GHz ISM Band. *Analog Integrated Circuits and Signal Processing*, 104(2), 317–325. https://doi.org/10.1007/s10470-020-01653-5

[7] Natarajan, K., & Srivastava, V. (2019). CMOS Power Amplifier Topologies for Energy-Efficient IoT Devices: A Review. International Journal of Electronics and Communications (AEÜ), 105, 45–55. https://doi.org/10.1016/j.aeue.2019.03.005

[8] Keysight Technologies. (2021). Fundamentals of Load-Pull Measurements. Application Note. https://www.keysight.com/

[9] Kang, S., & Ryu, Y. (2020). High-Efficiency Class-E CMOS Power Amplifier with Harmonic Suppression for IoT Applications. Journal of Semiconductor Technology and Science, 20(5), 456–462. https://doi.org/10.5573/JSTS.2020.20.5.456