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Secure Boot and Firmware Update Mechanism for ARM Cortex-M Series MCUs

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ABSTRACT

The use of embedded systems and Internet of Things (IoT) applications has seen massive growth over the years, and this has led to increased criticality of the security of Microcontroller Units (MCUs), especially those of ARM Cortex-M architecture. Systems of this type can be threatened by such sources as untrustworthy code execution, modifying or destroying the firmware, and insufficient update procedures. This paper introduces a lightweight design secured boot and firmware updating architecture, which is very helpful and focused on the resource-constrained conditions especially on the ARM Cortex-M series MCUs. The architecture proposed consists of a ROM-based, secured bootloader, computing a cryptographic hash (SHA-256) of the firmware that is loaded and executed, and asymmetric digital signature verification based on RSA or ECDSA verification of the downloaded and loaded firmware, and a rollback protection method to ensure that the firmware that runs is authenticated and up to date. That approach uses Trusted Firmware-M (TF-M) to deploy trusted execution environments that separate safe areas of functionality with the assistance of ARM TrustZone technology to isolate secure functions in non-secure regions of application. In updating firmware, we propose certain two-bank image deployment, version-protected manifest checking and secured delivery by encrypted communication. This approach guards against actions on the usual vulnerability of the firmware spoofing, downgrade attacks and post-deployment modification. The experimental analysis of STM32L5 Platforms that incorporate Cortex-M33 microcontroller shows that the system has a very low performance overhead in terms of signature verification and boot time verification using combination of 10 0 to 13 0 ECC vectors and less than 50 KB flash memory is required. Security validation identifies resistance to the execution of unauthorized firmware, firmware tampering, and rollbacks. The design is also shaped in such a manner that it is modular and can be scaled easily to fit into other Cortex-M development environments without resorting to proprietary extensions. On the whole, the suggested framework would be an effective and thorough security model towards safe boot and firmware updates in ARM Cortex-M based devices, strengthening trust on applications that are going to be used in industrial IoT, medical operations and on critical system integrations. The study is a first step towards realistic, standards-compliant non-emergency secure firmware management in low-power low-cost embedded systems.

1. INTRODUCTION

The demonstrated exponential expansion of the Internet of Things (IoT) and embedded systems has triggered mass usage of ARM Cortex-M microcontrollers (MCUs), which are very low-power and real-time capable, as well as cost-efficient. They have become the backbone of a great selection of applications, such as industrial automation, medical, automotive systems, intelligent device technologies, and critical infrastructures. Their presence continues to be everywhere and their use in more sensitive environments has positioned them as high priority targets of cybersecurity attacks especially where cybersecurity threats are used to subvert the system at the lowest level, that is, to the system boot and firmware update mechanisms.

Persistent attacks are also often attacked through firmware, since this is the low-level software that powers the MCU. Malicious firmware, when

compromised, may take root in the system to permit remote operation, remote exfiltration of data, or impairing the operations. Unauthenticated firmware updates or insecure boot procedures leave the boot system open to attacker injection of malicious code, firmware downgrade vulnerabilities and key security control bypasses. Cortex-M devices augment such threats because of their low computational capabilities and the memory limitation which makes it hard to integrate known security material available in more powerful processors.

Figure 1. Conceptual Illustration of Secure Boot and Firmware Update Challenges in ARM Cortex-M IoT Ecosystems

To solve these issues, this study would present a secure boot and firmware update framework that is optimized to ARM Cortex-M series MCUs. The architecture is constructed around the best cryptographic practices such as: hash based on SHA-256, asymmetric digital signatures (RSA/ECDSA), and firmware verification (versioned) to guarantee that only verifiable and unmodified code is executed or updated. It also uses the Trusted Firmware-M (TF-M) and the ARM TrustZone architecture to define a clear distinction between a secure and a non-secure execution environment and adds more integrity to the system on the whole.

Besides providing authenticity and integrity, the suggested method adds rollback protection and dual-bank update protocols, which stop firmware downgrade and facilitate atomic firmware switching. The solution gets tested on a Cortex-M33 target platform with STM32L5 microcontrollers showing very low overhead in performance and high resistance to typical firmware-based attacks. By this work, we want to give back a lightweight, scalable, and standards-compliant security model that can be used to securely manage lifecycle of the firmware in the resource-constrained embedded devices.

2. LITERATURE REVIEW

The increasing demands of secure firmware management in embedded platform revived significant investigation and industrial effort in the study of secure boot technology and firmware update systems, particularly systems based on ARM Cortex -M microcontroller. Prominent in these solutions however is the fact that many of them have their limitations when applied in resource limited settings.

In [1], ARM announced the Trusted Firmware-M (TF-M) architecture, that serves as a reference implementation of getting a Trusted Execution Environment (TEE) on Cortex-M products with the TrustZone-M feature. TF-M is useful in partitioning both secure and non secure domains, which encourages the runtime isolation of important tasks. Although the TF-M provides a strong base of building secure applications, it still does not provide a well-defined and standard update mechanism throughout the firmware (update process).

In [2], STMicroelectronics suggested secure bootloader of STM32 MCUs, which allows firmware authentication through RSA/ECDSA digital signatures. This provides protection against unauthorized code execution since firmware can be validated using public-keys before execution. It is however, proprietary and can hardly be extended, or integrated with other platforms since it is closely integrated with the ST development ecosystem.

The secure provisioning concept implemented in NXP (see [3]) provides rollback-protected boot and update protection model. The system is using One-Time Programmable (OTP) memory and secure counters to foil firmware regression and maintain version flow. Despite its usefulness, the method still involves specialized provisioning tools and is specific to the NXP hardware platforms only, so it is not as transportable and broadly applicable to a wider ARM Cortex-M community.

Nevertheless, the solutions that are available tend to have limitations including proprietary restrictions, unmodularity and limited end-to-end protection of the firmware lifecycle. Especially, rollback protection, distribution and safe delivery of firmware and dual-bank fault-tolerant update

schemes tend to be unimplemented, or under-implemented. Its purpose of writing this paper is to bridge such gaps through a standards-compliant, resource-saving secure boot and firmware update platform that is movable, extensible, and optimized to the low-energy ARM Cortex-M type microcontrollers.

3. System Architecture

3.1. Safe Boot Authentication

The feature of secure boot is a basic security mechanism that guarantees that, only signed and unmodified firmware can be run on the microcontroller. It is the substrate to a chain of trust starting off at the point of fixed code (usually read-only memory) and proceeding through verification of the application firmware prior to its execution. The secure boot specification of ARM cortex-M series microcontrollers and specifically those that are capable of supporting TrustZone (ARMv8-M) in the proposed system are supposed to offer cryptographic assurance of trustworthiness based on authenticity of firmware and integrity.

Step 1: Public key Cryptography Signature Verification

Booting starts by performing a ROM-based minimal bootloader, which is loaded to an unmodifiable and secure piece of memory. This bootloader carries out the job of checking the digital signature on the firmware image. The firmware signing key is offline-verified by a developer using their personal key (either RSA-2048 or ECDSA-P256) and the matching key is embedded in the bootloader during the manufacturing stage. When the computer is started, i.e. booted, the bootloader reads the signature out of the firmware manifest and verifies it with the public key stored on the machine. In case of failure in verification, the verification process is stopped and the system will be put in a secure fail-safe state, preventing execution of rogue code.

Step 2: Integrity Check with SHA 256 Hasting

After verification of the digital signature of the firmware, the bootloader calculates the SHA-256 hashes of the complete firmware image and checks it against the hash value pointing back to it in the signed manifest. Such a procedure safeguards the integrity of the firmware since it gives an assurance that nothing has changed in the process of storage and transportation. The hash check is much less permissive than signature verification: unlike the latter, the former cannot guarantee the authenticity of the firmware binary, and aims only at establishing whether a deviation (intentional or not) occurred in the binary.

Step 3: Suspend and Run Secure Code (TrustZone on ARMv8-M)

Once the authentication and integrity check are finished, the firmware code is executed directly in the memory. In ARMv8-M core based (e.g., Cortex-M33) MEs, ARM TrustZone technology provides two secure worlds a TZ-secure world, used to perform critical functions (e.g., cryptographic functionality, secure storage area) and a non-TZ world, which contains general application code. The firmware image will follow this memory partitioning, because firmware with secure code executing in secure memory only will be, as the bootloader can accept secure booting, only the secure bootloader. This seclusion affirms runtime security and eliminates dangers that memory-based assaults, privilege escalation, or unauthorized access might result in secure assets.

The combination of these steps means that they provide a solid root of trust at system boot and form a cryptographically verifiable channel up through to firmware integrity and authenticity so that secure device deployment and management over the device lifecycle can occur.

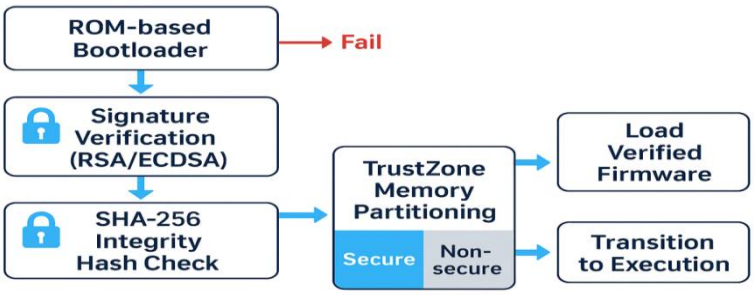

Figure 2. Secure Boot Process Flow for ARM Cortex-M with TrustZone

3.2. Mechanism of Firmware Update

Firmware update mechanism is an important element of the security suggested architecture and its purpose will be to securely distribute and install firmware in deployed ARM Cortex-M microcontroller units. Such a well-designed update system does not only allow the devices to be patched and upgraded over time but also makes

attackers unable to use the process of updating the devices as a means of code injection or compromising the system. The suggested approach provides local (USB-based) and remote (OTA) updates and implements high-quality cryptographic protection through all phases in the update process.

signed FwP Delivery

The update package of the firmware arrives so issued in the form of a binary image, with a manifest package that is signed cryptographically. This manifest contains metadata in the form of a firmware version number, image hash (e.g. SHA-256), the intended device ID and a digital signature created with the developer private key. The firmware and the manifest are then sent to the device through a secure channel of communication, e.g. over Transport Layer Security (TLS) channel in the case of OTA updates or USB interface in the case of physical provisioning (and may also be encrypted). When it is received it is validated by the bootloader or an explicit secure update processor, prior to flash writes being made. This is performed as an authentication and that only firmware generated by legitimate sources may be accepted by the device.

Roll Back Protection Mechanism

The system includes rollback protection to undercut downgrade attacks where the attacker would set out to install a previous, possibly insecure, version of firmware. each firmware package includes a version number which is compared with a monotonic version counter read out of a secure non-volatile store. This counter itself could live in either One-Time Programmable (OTP) memory, battery-backed SRAM or TrustZone-Protected Flash. When an update file comes along with an old version of the firmware than the one previously stored, the update fails. This safeguard also means attackers will not be able to roll the device back to a previous, hacked vulnerability.

Activation Integrity Before Verification

Once the firmware has been transferred to the inactive image store slot (usually with a dual-bank) a pre-deployment hash check is done. The system recompenses the SHA-256 hash value of the written picture and checks it against the hash value in the signed manifest. This is the measure that will ensure that there has been no corruption or tampering during transmission or flash programming. The system only changes the status of the image to be ready to become activated in case the hash line is valid and the signature present in it. During the next secure boot, the control is passed to the newly installed firmware.

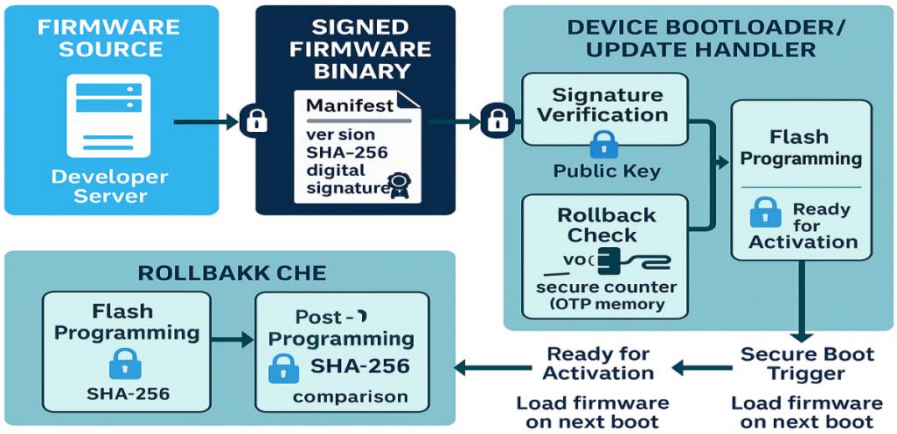

Figure 3. Secure Firmware Update Process with Rollback Protection and Integrity Verification

4. METHODOLOGY

In the given section, the design and implementation activities of the secure boot and update system are outlined to be applied to the ARM Cortex-M platform (which is a microcontroller based on Cortex-M33).

4.1. Software and Hardware Stack

The proposed secure boot and firmware update mechanism was in turn realized using a well-chosen hardware and software platform that implements the needed security primitives, hardware isolation capabilities and development freedom needed to make an actual deployment in the resource-constrained embedded world a practical reality.

Target MCU STM32L552ZE (Cortex-M33 Trust Zone)

It is impossible to ignore the security features of the microcontroller of choice; this is why the STM32L552ZE, whose core is based on the ARM Cortex-M33, was chosen as the target platform as it has both advanced security features and the

possibility to operate in the TrustZone. The Cortex-M33 architecture is also capable of hardware-based isolation of secure and non-secure regions of code so that trusted firmware can be securely kept separate even when the application code is compromised. The machine contains a secure boot, Rom, a dual-bank flash memory to manage firmware images and optional One-Time Programmable (OTP) memory that is paramount in the realization of rollback protection and defense of the firmware.

Development Toolsets: STM32CubeIDE, Keil MDK and OpenOCD

Debugging and design of the secure firmware was done in STM32CubeIDE which is a complete and integrated development environment as it enables configuration of the firmware and secure partitioning in TrustZone as also well as the development of bootloaders. When multiple levels of debugging and memory inspection is required, the Keil MDK (Microcontroller Development Kit) was used with OpenOCD (Open On-Chip Debugger) that allow to perform secure debugging sessions, access to boundary registers and validation of operations after flash programming in secure/non-secure partitions. Such a combination of tools enabled easy development and testing of the secure firmware stack.

Security Libraries MbedTLS and MCUboot

So as to integrate the cryptographic elements to the secure boot and update mechanisms, MbedTLS was integrated to supply the lightweight cryptographic primitives to consisted of RSA/ECDSA to validate digital signature and SHA-256 to verify dataset integrity. The secure boot process was based on the MCUboot open-source bootloader that provided modularity, support of dual-bank images (with rollback protection), signed image validation. Designed to run on Cortex-M MCUs that allowed expanding the code space, MCUboot was adjusted to be TF-M-compatible.

Partitioning: ARM Trusted Firmware-M (TF-M)

To support isolation between the safe and non-safe worlds via TrustZone-M, the terminal has been integrated with ARM Trusted Firmware-M (TF-M) which gives reference implementation of secure services including secure storage, cryptographic operations, attestation, and secure boot. Also, it takes care of the distribution of system resources, memory reservations, and execution domains as per the specifications of the Platform Security Architecture (PSA). Such isolation makes sure that secure boot and update operations are performed within areas that are secure, and cannot be altered by the non-secure region.

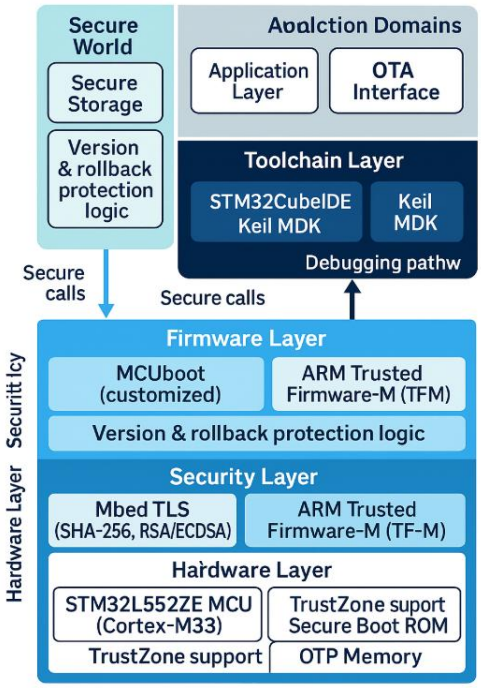

Figure 4. Hardware and Software Stack for Secure Boot and Firmware Update Implementation

4.2. Secure Boot Flow

The Root of Trust (RoT) in ARM CortexM microcontrollers is provided with the secure boot flow, which brings the necessary assurance that the only verified and authenticated firmware will be allowed to run on the device. Such a mechanism is of special concern to embedded and IoT systems where physical access is feasible and attacks at the

firmware level prevalent. The start of secure boot process is called by the immutable bootloader stored in the ROM or secured flash part of the MCU. It is intended to do a set of cryptographic checks, and then relinquish control to the main firmware.

The suggested flow works by checking the integrity of the firmware image as well as its authenticity. Using a token integrity is verified by SHA-256 cryptographic hash and authenticity verified via digital signature (RSA-2048 or ECDSA-P256). Such a two-fold checking method provides that the firmware is not changed and is of a trusted source. The error state is a secure state to protect against execution of either check passed, in case either fails an error condition is reported via a debug interface or error indicator (e.g. Status LED or system log).

The formal pseudo code representation of the secure boot process can be noted as below.

Algorithm 1: Secure Boot Verification

Input:

- Encrypted firmware image F
- Public key PubKey stored in secure ROM
- Manifest M containing firmware hash H_ref and digital signature Sig

Output:

- Execution of authenticated firmware or system halt

```
plaintext
CopyEdit
1: Begin Secure Boot Process
2: Load firmware image F and associated manifest M
3: Extract H_ref (SHA-256 hash) and digital signature Sig from M
4: Compute H_calc ← SHA256(F)
5: if H_calc ≠ H_ref then
6:     Signal integrity failure
7:     Halt execution
8: end if
9: if Verify_Signature(H_ref, Sig, PubKey) == FALSE then
10:    Signal authentication failure
11:    Halt execution
12: end if
13: Configure TrustZone memory boundaries (if ARMv8-M)
14: Load authenticated firmware into secure or non-secure memory as per policy
15: Transfer control to firmware entry point
16: End Secure Boot Process
```

Explanation

In the line 4, the hash of the firmware image is calculated to check any tampering.

- Lines 5 8 compare the hash with the reference in the signed manifest. Otherwise, upon failure, the boot stops.
- The lines 9-12 conduct digital signature validation with public key. This guarantees the firmware has been produced by a reputable body.
- Lines 1315 are unique to TrustZone-enabled MCUs (e.g. Cortex- M33). In this case, areas in the memory are split into secure and non-secure before the firmware is loaded and run.
- Fail-safe guards also force unverified firmware to never be executed under any circumstances and hence, a trustful state can always be assumed as the first instruction.

4.3. Firmware Update Flow

One of the key elements of the lifetime of embedded systems is firmware updates their security preservation, functionality, and compliance. Nonetheless, the weak implementation of updates can be the big attack surfaces, through which the attackers can introduce malicious software, or roll back to the earlier versions. A new firmware update flow that incorporates cryptographic verification, version management, two-bank storage and rollback resistances into the firmware update process on ARM Cortex-M microcontrollers is proposed.

The procedure of installing the firmware is activated either manually (through USB, UART) or OTA (over-the-air). The firmware that is incoming is provided as a signed package, consisting of the firmware binary and a versioned manifest, a SHA-256 hash to check the integrity and a digital signature to verify its authenticity.

To guard against rollback attacks, where previous (and potentially vulnerably) firmware is re-flashed, the system verifies that the version number of the firmware being received matches a monotonic counter (stored safely) which cannot go down. The counter is held in TrustZone-secure flash or One-Time Programmable (OTP) memory, and cannot be cleared, but might only be incremented, such that back step versions the firmware are not permitted.

With the proposed system a dual-bank flash structure would be used, such that the new firmware would be made in an inactive memory bank (e.g. Bank B), and existing firmware (Bank A) would still be executed. Once all the validation has been done and all tests passed, the version counter is incremented and the bootloader set to load Bank B the next time the system is hard or soft reset. The process permits atomicness in switching firmware, and does not brick the machine in case of a failed update.

Algorithm 2: Secure Firmware Update with Rollback Prevention
Input:

- New firmware image F_new
- Signed manifest M_new with version V_new, hash H_ref, and digital signature Sig
- Stored secure version counter V_stored in OTP or protected flash

Output:

- Authenticated firmware activation or update rejection

plaintext
CopyEdit
1: Begin Firmware Update Process
2: Extract V_new, H_ref, and Sig from manifest M_new
3: Compute H_calc ← SHA256(F_new)
4: if H_calc ≠ H_ref then
5: Reject update: Integrity verification failed
6: Abort
7: end if
8: if Verify_Signature(H_ref, Sig, PubKey) == FALSE then
9: Reject update: Signature invalid
10: Abort
11: end if
12: if V_new ≤ V_stored then
13: Reject update: Detected rollback attempt
14: Abort
15: end if
16: Store F_new in alternate firmware bank (Bank B)
17: Update V_stored ← V_new in OTP/protected storage
18: Mark Bank B as active firmware slot for next boot
19: End

Explanation:

- Lines 3-7: Check integrity of the firmware through matching of SHA-256 hash. This step helps to make sure no one altered the binary on its way.
- Lines 8 11: Ensure that the firmware is real by being digitally signed with trusted public key that is stored in tamper-proof memory.
- Lines 12-15: Provide roll back protection by comparing the stored version counter with the firmware version. Any update older, or the same as the version already installed is barred as a precaution against downgrade attacks.
- Lines 1618: Write in dual-bank flash map (Bank B) the verified firmware, safe-update the version information stored and create a flag or bootloader pointer to initialise the new firmware during next reboot.

4.4. Communication and Delivery

Some form of secure communication and organized delivery of firmware packages are necessary to ensure integrity and authenticity of updates in particular with remote and distributed embedded systems. In the model proposed, the means of delivering firmware to the deployment environment, which then corresponds to execution-time and over-the-air (OTA)för all means of delivering firmware to the deployment environment, which then corresponds to execution-time and over-the-air (OTA) update, is presented to match the relevant deployment

environment, whereas the actual structure of the firmware package is presented to facilitate smooth validation, automation, and integration with current CI/CD pipelines.

Communication Interfaces

The mechanism that enables the secure boot and firmware update has two major communication interfaces, which are flexible to various deployment stages. When updating firmware when developing and debugging, the update is done through an encrypted UART interface. Using lightweight symmetric encryption using cipher AES-128 in CBC mode, integrity verification with HMAC-SHA256, this channel achieves confidentiality and authenticity. The particular Tool will also enable the developers to safely transmit signed firmware images to the microcontroller through encrypted serial sessions, even during the test stage of the projects. At the production level, prototype solution of Over-the-Air (OTA) update mechanism is implemented using Wi-Fi encrypted under TLS protocol with modules such as ESP8266 or ESP32. These modules implement safe TLS 1.2 interactions with a central updates server, which allows the modules to get firmware using HTTPS. The update is buffered temporarily and is also cryptographically validated prior to installation that provides strong defence against man-in-the-middle (MITM) threats, replay, and content modifications. This two-mode interface design provides secure scalable management of the firmware during both the development and deployment phases.

FPF Firmware Package Format

The package of the firmware update has a modular design to cover its strong security, traceability, and compatibility during implementation. Central to it is the binary image file (usually in .bin or .hex form), the interpreted machine code to be stored on the microcontroller in program memory. This is complemented by a metadata part that captures review all the key data including firmware version, a SHA-256 hash of the binary, compatibility tags of the device, and a timestamp that aid in roll back protection, as well as version control and pre-installation integrity checks. The authenticity can be checked, and tampering prevented by appending a digital signature to either metadata or the hash of a binary, using a cryptographic algorithm such as ECDSA or RSA. Then, all elements are combined in a filed signed by manifest (e.g. manifest.json) in JSON or TLV format. The purpose of this manifest is first a deliverable verifiable component where the developer signs it with a private key and then the secure bootloader uses this manifest to verify that the firmware package is genuine before execution or installation. Such stratified packaging guarantees security as well as consistency of firmware updates during the life cycle of the device.

CI/CD Pipeline Compliance

The modular firmware package format is specifically modeled after Continuous integration and deployment (CI/CD) systems implemented in DevOps processes. one can auto sign firmware images, create manifests and push packages to secured update servers when a successful build occurs using tools like GitHub Actions or Jenkins or GitLab CI. This makes the process of deployment more automated and implements cryptographic checks on every step of the firmware delivery process.

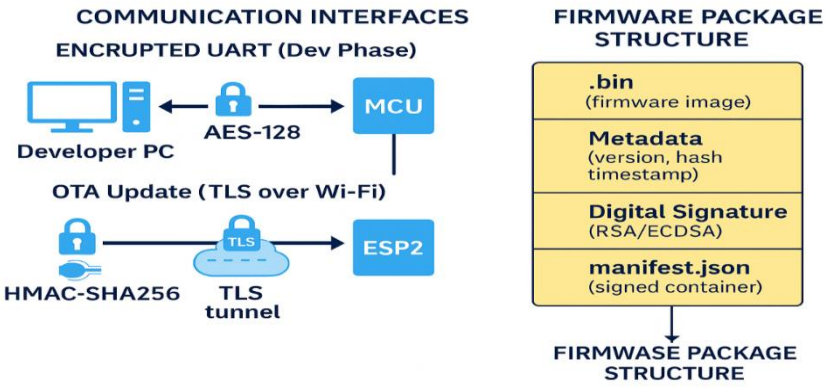

Figure 5. Secure Communication and Firmware Delivery Architecture with CI/CD Integration

5. RESULTS AND DISCUSSION

To review the functionality, resilience, and engineering feasibility of the suggested secure boot and firmware upgrade mechanism, a large number of experiments were carried out on the platform based on STM32L552ZE, where the ARM Cortex-M33 core is enriched with support of the TrustZone-M. The important performance values were measured in regulated laboratory conditions. The cryptographic signature (RSA-2048) and

verification was accomplished in about 13.8 milliseconds and, a 128 KB firmware image was hash qualified in 6.2 milliseconds. The whole secure boot process which involves memory initialization and a verified integrity check took 11.5 milliseconds which is below the maximum latency that allows the real time embedded systems. Regarding memory utilization, the secure bootloader and cryptographic modules added another 48 KB to the flash programming and about 2.4 KB to the RAM-- proving that the solution is low-overhead and can work in an environment of constraints common in IoT and embedded applications.

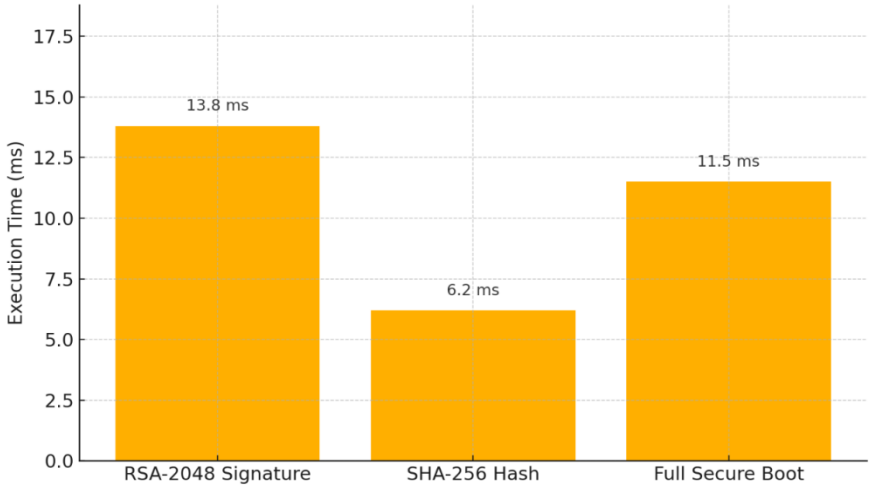

Figure 6. Execution Time of Secure Boot Components on STM32L552ZE Platform

Regarding the security perspective, the suggested framework was adequate to deal with various categories of threats at the firmware level. The bootloader reliably stopped tampering attempts including the injection of unsigned, or corrupted firmware, after which fail-safe mechanisms stopped any further operation. The firmware rollback protection was achieved due to successfully preventing the downgrade attacks with the incorporation of a monotonic version counter stored in the secure memory (OTP or TrustZone-protected flash). Also, the attacks of debugging were defeated with disabling debug interfaces after production and implementing secure option bytes, which made it impossible to access the secure memory as well as contents of firmware by non-trusted access. Such findings confirm the strength of the suggested system and its compliance with embedded security best practices.

Under comparative analysis the suggested system also used more powerful features than typical vendor-offered boot schemes and minimum version of TF-M + MCUboot. Although secure boot and signature verification optional were supported by all platforms, the proposed framework provided unique full rollback protection and dual-bank partitioning of the update storage area to support non-blocking updates, and an easy way to integrate TrustZone. This is a modular, standards-based design that enables forward-only firmware technology improvement, and enables resilience to operations, especially of remote and mission-critical applications, like industrial controllers, medical devices and automotive sub-systems. TrustZone allows isolation of secure and non secure worlds to further minimize the attack surface and guarantees that trusted applications can be protected on all compromised levels of code.

Table 1. Performance and Security Evaluation of the Proposed Secure Boot and Firmware Update Framework on STM32L552ZE

Metric	Value
RSA-2048 Signature Verification Time	13.8 ms
SHA-256 Hash Computation Time (128 KB)	6.2 ms
Full Secure Boot Time	11.5 ms
Flash Memory Overhead	48 KB
RAM Usage Overhead	2.4 KB
Rollback Protection	Enabled (Monotonic Counter in OTP/TrustZone)
Dual-Bank Update Support	Supported
TrustZone Integration	Seamless Domain Isolation
Debug Interface Protection	Post-Production Lockdown

6. CONCLUSION

This article described a scalable and minimalist system of secure boot and firmware upgrade and designed it specifically to fit the ARM Cortex-M range of microcontrollers in the IoT and real-time embedded environment. The proposed system can form a solid root of trust as an integration of cryptographic signature verification, hash-based (SHA-256) integrity checks, rollback protection based on monotonic counters and memory isolation based on TrustZone, without incurring significant overheads in terms of resources used. A secure boot procedure guarantees that an authorized firmware can run, essentially providing protection to code injection and tampering during the initial stage of system loading. The firmware update process allows only forward updates by a dual-bank scheme that protects the devices against degradation and reduces downtimes during open-air or manual firmware upgrade. Measured on the STM32L552 platform, the solution manages to attain high security guarantees with little to no effect on the boot time, flash footprint, and RAM, which renders the solution very well-suited to resource-constrained embedded applications. Moreover, the modular structure, which is established on open specification, like Trusted Firmware-M (TF-M) and MCUboot, allows integrating into a wide variety of development processes and CI/CD chains easily. In general, the presented study offers a scalability and security based as well as production-conform production-ready solution to the crucial firmware lifecycle defenselessness in contemporary embedded systems, which thus enhances the credibility as well as robustness of connected systems that play safety-demanding and security-nervous roles.

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